An Electronically Tunable Capacitance Multiplier Employing Single Active Block For The Speech Processing Applications

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Abstract

In this work, a novel capacitor multiplier based on the Current Difference Transconductance Amplifier (CDTA) is introduced and constructed by using NMOS and PMOS transistors. The CDTA-based design integrates two primary stages: a Current Follower and a Dual-Output Operating Transconductance Amplifier (DO-OTA). Operating within a ±0.9V range, the structure particularly features a PMOS transistor functioning between -0.5V to -0.9V. Notably, the capacitor multiplication factor exhibits tunability via the PMOS gate voltage, targeting low-frequency operations where large capacitor values are in demand. Performance investigation of the multiplier is given in basis of a 2nd order low-pass filter, revealing a cut-off frequency ranging from 2.7 kHz to 7.1 kHz, suitable for the speech processing applications. The filter's power consumption is found as 1.5 mW. Furthermore, by changing the V_{GS} of the PMOS, the multiplication factor varied from 120 to 300. To evaluate the robustness and efficacy of the design, a set of analyses are presented, including Monte-Carlo simulations, total harmonic distortion (THD) measurements, and noise assessments with the filter performance outcomes. A comparative analysis shows the improvements of the proposed design over the previous studies.

Keywords: CDTA, Capacitor Multiplier, Speech Recognition, DO-OTA, Low-pass filter.

1. Introduction

In recent decades, there has been a marked surge in the demand for portable and wearable technologies. Such technologies encompass a broad spectrum, ranging from smart watches to diverse wireless devices common in modern consumer electronics [1,2]. Beyond traditional consumer utilities, speech recognition has emerged as a critical application, driving innovation and necessitating specific device requirements [3]. Speech recognition systems, especially in portable formats, demand high computational capabilities while being constrained by limited power budgets and form factors. All these factors listed herein collectively constitute the motivation for the inception of this study.

To address the challenges of minimal chip real estate, capacitor multipliers have been extensively explored [4,5]. By employing feedback mechanisms, these multipliers have demonstrated enhanced multiplication factors in both voltage and current mode designs [6,7]. In previous studies, active elements such as OTA, OPAMP, DVCC, CDTA, CFTA and VDTA have been integrated into capacitor multipliers to achieve desired performance metrics [8-16]. Meeting these requirements presents a unique set of challenges but also opens the door to countless opportunities in creating efficient, responsive and user-friendly interfaces.

It is necessary to underscore that these advanced devices often necessitate specific design criteria, particularly in the studies of low voltage, low power consumption, and minimized form factor to ensure optimal performance and user convenience.

In the studies of multiplier studies, designs can predominantly be categorized into voltage and current modes [4-15]. Specifically, within current mode designs, the multiplication factor, denoted as "k", modulates the base capacitance as per the relation "$C_M = (1 + k)\, C_B$". In this equation, "C_B" represents the based capacitor value, whereas "C_M" gives the enhanced capacitor value.

It is mandatory to highlight that the primary objective of this study is to achieve significant capacitance values crucial like as speech recognition functionalities operating at low frequencies in wearable devices, all while ensuring minimal power consumption. In this context, various methodologies have been proposed like as reducing the power supply requirements, tunability of multiplication factor, and working with specific frequency intervals [17].

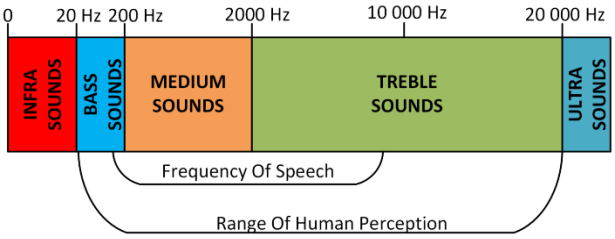

Fig. 1. Frequency Interval Of Voices

This paper introduces a tunable capacitance multiplier realized through the use of CDTA as a primary active block. The design was entirely realized using TSMC 0.18µm CMOS technology. One of the critical features of this research is the capability of achieving multiplication factors coupled with minimal power consumption in specific frequency intervals. The multiplication factor is tunable, ranging from 120 to 350, based on the V_{GS} voltage of external PMOS.

The proposed capacitance multiplier architecture is based on a CDTA, harmonizing performance, and efficiency. To verify the multiplier impact, a 2nd order low-pass filter, adapted for low-frequency applications, was introduced as a demonstrative application. Comprehensive Monte-Carlo and temperature analyses were conducted to validate the multiplier robustness across varied operating scenarios. A noteworthy finding was the adjustability of the "k" multiplication factor in conjuction with the V_{GS} of external PMOS, which ranged from -0.5V down to -0.9V. The entirety of the simulations was executed within the LT-Spice environment, ensuring consistent and reproducible results.

The organization of this paper is articulated as follows: Section II explores into the characteristics of CDTA, establishing its foundational role within the proposed design. Section III defines the proposed capacitance multiplier. Section IV presents a comprehensive set of simulation results for the proposed structure, providing empirical evidence of its performance. This section also incorporates a comparative analysis, compared studied work against previously studies to highlight advancements and improvements. Concluding remarks and potential future directions are summarized in Section V.

2. Characteristics Of CDTA

The Current Differential Transconductance Amplifier (CDTA) provides as a fundamental building block in designs based on active elements. Conventional CDTA configurations are typically characterized by the integration of two blocks. Current Follower stage and Dual Operational Transconductance Amplifier (DO-OTA) blocks can be given as explained in [15]. A block representation of the CDTA can be found in the Fig.2. The generalized characteristics of CDTA are giaven Eq.1.

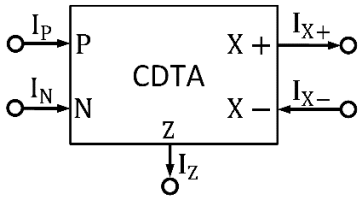

Fig. 2. Block Representation Of CDTA

$$\begin{bmatrix} V_P \\ V_N \\ I_Z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_X \\ V_Z \end{bmatrix} \quad (1)$$

The complete architecture of the CDTA is represented in Fig. 3. Fundamentally, the CDTA occurs two primary modules: the current follower block and the DO-OTA configuration. The entire block diagram experienced modifications customized to the capacitor multiplier structure. To achieve optimal performance, the W/L ratios of the circuit were carefully determined. These W/L ratios for each transistor are represented in Table 1. The proposed CDTA architecture contains two seperate current sources, with each providing to a unique structure. It's remarkable that the current I_B is lower than I_C. The W/L ratios of the CDTA have been carefully determined to align with the design specifications of the proposed configuration.

Table 1. Dimensions Of Transistors

TRANSISTOR	Dimensions	
	W	L
M_{1B}	1 µm	0.36 µm
$M_{2B}, M_{3B}, M_{4B}, M_{5B}$	2 µm	0.36 µm
$M_{6B}, M_{7B}, M_{8B}, M_{9B}$	6 µm	0.72 µm
M_1, M_2, M_3, M_8	1.5 µm	0.36 µm
M_4, M_7, M_9, M_{10}	3 µm	0.36 µm
M_5, M_6	6 µm	0.36 µm
M_{1C}, M_{2C}	9 µm	0.36 µm
$M_{3C}, M_{4C}, M_{7C}, M_{8C}$	54 µm	0.36 µm
$M_{5C}, M_{6C}, M_{11}, M_{12}$	20 µm	0.36 µm
M_{13}	10 µm	0.36 µm
M_{14}	18 µm	0.36 µm

3. Proposed Capacitor Multiplier

The block diagram of the proposed capacitor multiplier is represented in Fig. 4. This design functions effectively as a current mode capacitor multiplier. As illustrated in Fig. 4, a current determined as “k.I” crosses the feedback loop, while the base capacitance is primarily engaged by a current magnitude of “I” [6].

A significant feature of the proposed architecture is its tunability, facilitated by the V_{GS} voltage of the external PMOS. This PMOS provides the R_O resistor within the circuit. It is relevant to note that the R_O value is adjustable and dependent on the V_{GS} voltage associated with the external PMOS.

Operating within the linear region, the behavior of the external PMOS can be mathematically expressed as detailed in Eq. 2 and Eq.3.

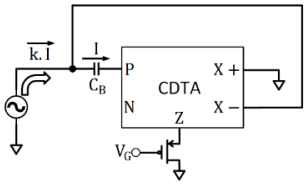

Fig. 3. Proposed Capacitor Multiplier

$$I_{SD} = \mu_P C_{OX} \frac{W}{L} [(V_{SG} - |V_T|)V_{SD} - \frac{V_{SD}^2}{2}] \quad (2)$$

$$R_O \cong \frac{1}{k_P \frac{W}{L}(V_{SG} - |V_T|)} \quad (3)$$

$$Z \cong \frac{1}{sC_B + sC_B g_m (R_Z // R_O)} \quad (4)$$

The impedance and multiplication factor of the proposed architecture are analytically expressed in Eq.4 and Eq.5, respectively. These mathematical representations were derived through strict analysis of both the block diagram and the internal configuration of the study. It is important to remember that these

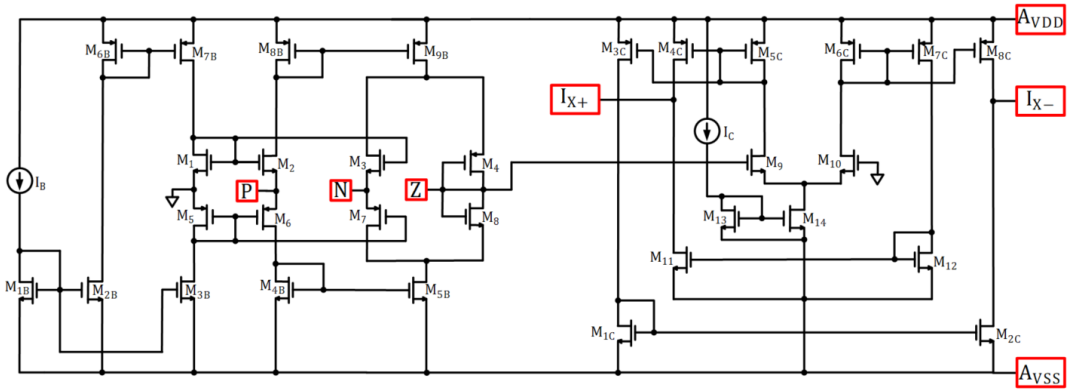

Fig. 4. CMOS Implementation Of CDTA

equations were provided without comprehensive parasitic effects of proposed structure.

$$k \cong 1 + g_m R_O \qquad (5)$$

4. Simulation Results

In the present study, simulation results are obtained using the LT-Spice tool based on the 0.18µm TSMC CMOS technology. The proposed structure is worked by supply voltages of ±0.9V, with the exception of the external PMOS transistor, which operates in the range of -0.5V to -0.9V. Moreover, the specified current values are denoted as $I_B = 2\mu A$ and $I_C = 30\mu A$.

For the CDTA configuration to function as an effective capacitance multiplier, it is critical for the structure to present stable current transitions across the X+ and X- terminals. At the same time, the Z terminal should have a high impedance value. The transition characteristics and impedance values of the proposed circuit are simulated in LT-Spice simulation tool.

The shown that proposed structure can be work robustneslly. The transconductance values of the CDTA are determined as $g_m = 1000\ \mu S$ corresponding to the bias currents of $I_B = 2\mu A$ and $I_C = 30\mu A$.

And impedance value of Z terminal is measured 550 kΩ from 1 Hz to 1 MHz. Additionally, $R_P = 7.2$ kΩ and $R_N = 5$ kΩ are measured from 1 Hz to 100 MHz.

The primary characteristic of the proposed circuit is its function as a capacitance multiplier. The multiplication factor is adjustable based on the V_{GS} voltage, which in turn modulates the R_O resistance component of the impedance at Z terminal.

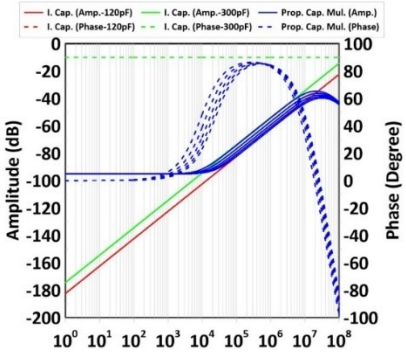

Fig. 5. Tunability And Multiplier Features Of The Proposed Circuit

As indicated in Eq.4, the R_Z value plays a significant role in influencing the multiplication factor. The factor can be adjusted robustly within a range of 120 to 300. This functionality is illustrated in Fig. 5. The variation due to temperature is depicted in Fig. 6. It is critical to note that the gain-frequency response of the proposed capacitance multiplier remains within acceptable limits when subjected to a temperature range changes from -40°C to +80°C. Both phase and amplitude responses exhibit minor deviations within this operating range.

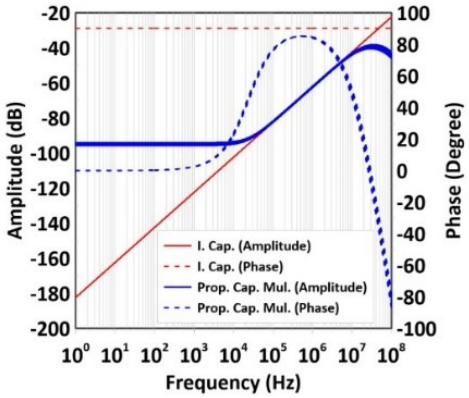

Fig. 6. Temperature Effect On The Capacitance Multiplier Characteristics

The filter application of proposed circuit is very important for demonstrate of success of the proposed structure. The different features of proposed circuit were investigated in different conditions. The capacitance multiplier based on CDTA implementation has been explored using a 2nd order filter, as represented in Fig. 7.

In this research, the multiplication factor, denoted as k, is adjustable, ranging from 120 to 300. With this consideration, when R_{IN} is set at 10 kΩ and V_{SG} voltage changes between -0.5 V and -0.9 V, the cut-off frequency of the 2nd order filter varies between 2.7 kHz and 7.1 kHz, as illustrated in Fig. 8.

Further, the filter exhibits a power dissipation of approximately 1.5 mW. Given its characteristics, the filter circuit proves to be operated for low-frequency applications such as speech recognition, where attributes like narrow bandwidth, minimal power consumption, and compact chip area are imperative.

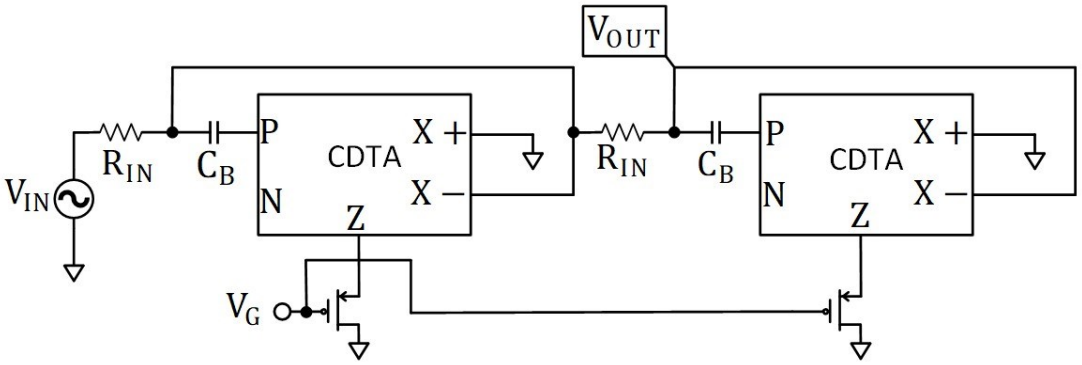

Fig. 7. 2^{nd} Order Filter Structure Based On The Proposed Multiplier Circuit

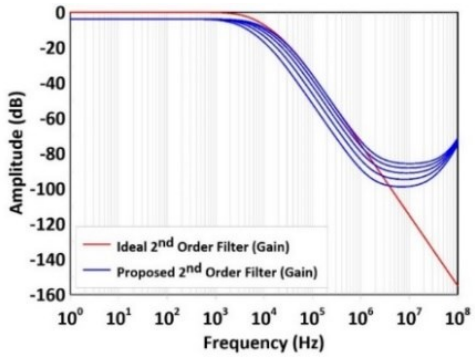

Fig. 8. 2^{nd}Order Low Pass Filter Response With Regard To Different V_{SG}

The other important point of proposed filter is temperature sensitivity. The sensitivity of proposed filter changes is in the acceptable bounds when temperature changes from -40 °C to +80 °C.

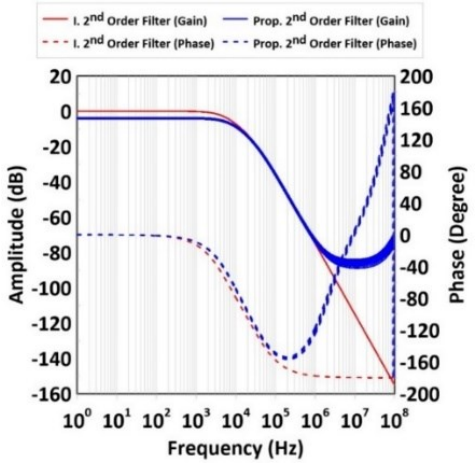

Fig. 9. Temperature Effect On The Proposed Filter

The linearity of the proposed 2nd order low pass filter can be verified by examining its transient response and total harmonic distortion (THD). Across a wide input amplitude spectrum, reaching up to 500mV V_p @1kHz, the THD remains within acceptable levels, below 3%.

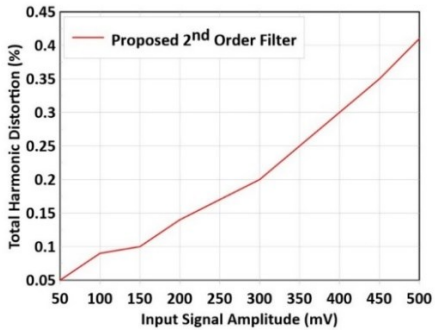

Fig. 10. THD Value With Regard To Input Signal

As the cut-off frequency transitions from 2.7 kHz to 7.1 kHz, the total input-referred rms noise shifts from 61.4 mV to 25.5 mV. A detailed representation of the input-referred noise behavior can be observed as given in Fig. 11.

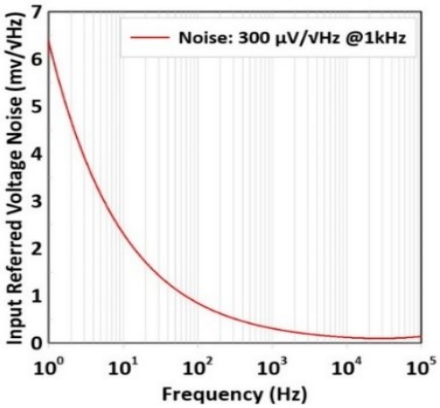

Fig. 11. Input referred noise behavior of the 2^{nd} order filter

The proposed second-order filter was subjected to testing using 100 independent Monte-Carlo seeds, varying passive elements and voltage supplies by ±10%. As illustrated in Fig. 12, the standard deviation of the filter's cut-off frequencies remains below 5%. Monte Carlo analysis was conducted to evaluate the lower and upper bounds of the cut-off frequency, demonstrating robust performance across diverse operating conditions.

Table 2. Comparative Analysis With The Previous Counterpart

Parameter	[6]	[8]	[9]	[11]	[12]	[13]	[14]	[16]	This Work
Publication Year	2013	2015	2022	2022	2022	2022	2019	2022	-
Technology (µm)	0.5	0.5	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Multiplication Factor (MF)	100	28	10-25.4	30–150	115-150	0-30	60-3600	10-10000	120-300
Base Capacitance (C_B)(pF)	10	25	10	10	1	NA*	3	50	1
P. Consumption (PC) (mW)	1.8	1.32	3.1	0.6	0.037	NA*	0.002	0.024	0.72
Operating Frequency Range (OFR)	1 Hz 1.5 MHz	10 kHz 1 MHz	1 kHz 100 kHz	10 kHz 10 MHz	10 kHz 200 kHz	NA*	5 kHz 1 MHz	1 Hz 30 KHz	10 kHz 8 MHz
# of Active Devices (AD)	1 FVF	2 OTA	1 VCII± 1 E-DVCC	1 CCCDTA	1 VDTA	1 CFDITA	1 OTA 1 CCII	1 ICFOA	1 CDTA
# of Resistance (NR)	0	0	0	0	0	2	0	2	0
Layout Area (mm^2)	NA*	0.14**	0.03**	0.01**	0.002**	0.0002**	0.0008**	0.0102**	0.004**
FoM	4.1	0.28	0.028	125	400	NA*	200 x 10^3	41	1600

NA: Not Available **: Approximated Layout Area: The summation of each transistor's area*

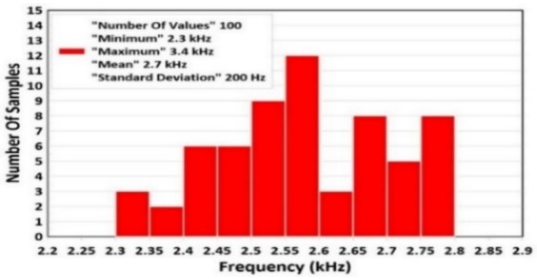

Fig. 12. Monte Carlo Analysis Of The 2^{nd} Order Low Pass Filter Lower Cut-Off Frequency

5. Conclusions

In this paper, a novel capacitance multiplier structure based on the Current Differencing Transconductance Amplifier (CDTA) is presented. Considered specifically applications demanding high capacitance values within a restricted layout, such as speech recognition systems, the proposed solution is fully realized using 0.18um TSMC CMOS technology and performed using LT-Spice simulations. Remarkably, the multiplication factor "k" can be tuned between 120 and 300 based on the Vgs voltage, while minimally affecting power consumption, which finds as low as 720 µW. Moreover, the structure adaptability for a 2nd order low pass filter, exhibiting cut-off frequencies ranging from 2.7 kHz to 7.1 kHz, underscores its potential for low-frequency applications, notably in the bounds of speech recognition systems. The comparative analysis as shown in Table 2, focusing on the Figure of Merit (FoM), further underlines its competitive performance. The chosen values for the Figure of Merit (FOM) have been selected with practical application in mind. Key parameters relevant to speech applications, namely OFR and MF, are specified in the numerator, while values associated with the area of layout and power consumption are placed in the denominator. It should be noted that the proposed circuit can be used for suitable frequency interval and multiplication factors in speech processing applications. Future works aim to enhance the multiplication factor while simultaneously optimizing power consumption and post layout analyses.

$$\text{FoM} = \frac{\max(\text{MF})\ x\ \text{OFR}}{PC\ x\ (AD{+}1)\ x\ (NR{+}1)\ x\ C_B}\left(\frac{MHz}{mW\ x\ pF}\right) \qquad (6)$$

6. References

[1] S. M. A. Iqbal, I. Mahgoub, E. Du, et al., "Advances in healthcare wearable devices," npj Flex Electron, vol. 5, no. 9, 2021.

[2] S. Seneviratne et al., "A Survey of Wearable Devices and Challenges," IEEE Commun. Surv. & Tut., vol. 19, no. 4, pp. 2573-2620, 4th quarter 2017.

[3] S. Furui, Digital Speech Processing: Synthesis, and Recognition, Second Edition. CRC Press, 2018.

[4] R. Sotner, J. Jerabek, L. Polak, and J. Petrzela, "Capacitance multiplier using small values of multiplication factors for adjustability extension and parasitic resistance cancellation technique," 2020.

[5] A. Shukla and P. Gupta, "Current-mode PMOS capacitance multiplier," in 2017 Int. Conf. on Inventive Systems and Control (ICISC), pp. 1–4, IEEE, 2017.

[6] I. Padilla-Cantoya, "Capacitor Multiplier With Wide Dynamic Range and Large Multiplication Factor for Filter Applications," IEEE Trans. on Circuits and Systems II: Express Briefs, vol. 60, no. 3, pp. 152–156, 2013.

[7] D. Biolek, J. Vavra, and A. U. Keskin, "CDTA-based capacitance multipliers," Circuits, Systems, and Signal Processing, vol. 38, no. 4, pp. 1466–1481, 2019.

[8] I. Padilla-Cantoya and P. M. Furth, "Enhanced grounded capacitor multiplier and its floating implementation for analog filters," IEEE Trans. Circuits Syst. II Express Briefs, vol. 62, no. 10, pp. 962–6, 2015.

[9] Ferri, G., Safari, L., Barile, G., Scarsella, M., Stornelli, V.: New Resistor-Less Electronically Controllable $\pm\mathcal{C}$ Simulator Employing VCII, DVCC, and a Grounded Capacitor. Electronics 2022, Vol. 11, Page 286. 11, 286 (2022). https://doi.org/10.3390/ELECTRONICS11020286

[10] Özer, E.: Electronically tunable CFTA based positive and negative grounded capacitance multipliers. AEU - International Journal of Electronics and Communications. 134, 153685 (2021). https://doi.org/10.1016/J.AEUE.2021.153685

[11] Ozenli, D., Alaybeyoglu, E.: An electronically tunable CMOS implementation of capacitance multiplier employing CCCDTA. AEU - International Journal of Electronics and Communications. 155, 154359 (2022). https://doi.org/10.1016/J.AEUE.2022.154359

[12] D. Ozenli, E. Alaybeyoglu, and H. Kuntman, "A tunable lossy grounded capacitance multiplier circuit based on VDTA for the low frequency operations," Analog Integr Circ Sig Process, 2022.

[13] A. Kumar, D. Singh, and D. Nand, "A Novel CFDITA-Based Design of Grounded Capacitance Multiplier and Its Transpose Structure," Circuits, Systems, and Signal Processing, vol. 41, 2022.

[14] M. A. Al-Absi and A. A. Al-Khulaifi, "A New Floating and Tunable Capacitance Multiplier With Large Multiplication Factor," IEEE Access, vol. 7, pp. 120076-120081, 2019

[15] Kacar, Fırat & Kuntman, Hakan. (2011). A new, improved CMOS realization of CDTA and its filter applications. Turkish Journal of Electrical Engineering and Computer Sciences. 19. 10.3906/elk-1003-467.

[16] Yucehan, T., Yuce, E.: A New Grounded Capacitance Multiplier Using a Single ICFOA and a Grounded Capacitor. IEEE Transactions on Circuits and Systems II: Express Briefs. 69, 729–733 (2022). https://doi.org/10.1109/TCSII.2021.3102118

[17] "Characterization of Sound," HearingProTech, [Online]. Available: https://www.hearingprotech.com/en/topics/noise/characterization-of sound.html.