Diode-connected transistor mixer analysis based on a linearized parametric model

Alexander S. Korotkov, Olga A. Golovan

Peter the Great St. Petersburg Polytechnic University, Polytechnicheskaya, 29, 195251, St. Petersburg, Russia
korotkov@spbstu.ru, golovan.olga.andreevna@gmail.com

Abstract

The current paper is a follow-up to the researches that deals with the frequency mixers analysis by the analytical method of nodal equations. The study considers the analysis of mixers, which circuit implementation includes diode-connected transistors (specifically balanced mixer, double balanced mixer and triple balanced mixer). Analysis of mixer characteristics such as conversion gain, port isolation (RF-IF and LO-IF), and mismatch effects are presented. A mixers parametric optimization using the criteria of conversion gain maximization is carried out. The results of analytical calculations and simulations in Cadence Design Systems are presented.

1. Introduction

In general case, frequency mixers are divided into two principal groups: active and passive. Active mixers are circuits based on the Gilbert cell. Depending on the operation mode of active elements, the authors emphasize four groups of passive mixers: current-driven passive mixers, voltage-driven passive mixers, diode mixers and passive mixers using diode-connected transistors. Active mixers based on Gilbert cell provide high conversion gain, however, have high noise figure, low linearity, and also high DC power consumption. Usually, Gilbert cell mixers are realized using CMOS technologies, and therefore they are used in L, S, C and X frequency ranges. Passive mixer circuits have certain advantages over active mixers: low DC power consumption, high linearity and low noise figure. However, the main disadvantage of passive mixers is the high conversion loss. Current-driven passive mixers and voltage-driven passive mixers are realized using CMOS-technology and are implemented in transceivers operating in L, S, C and X frequency ranges [1]. Diode mixers are realized on the GaAs-, SiC-technologies, that allows an extension their application to K and Ka frequency ranges [2]. Among passive circuit mixers using diode-connected transistors can be distinguished. This type of mixers is mainly realized using modern SiGe-technologies, that makes possible their application on V and W frequency ranges [3].

The relevance of passive mixers using diode-connected transistors practical application makes it necessary to develop methods of analysis and parametric synthesis of such type of mixers. In [4] a detailed review of existing methods of mixers analysis is presented, their advantages and disadvantages are determined. Also in [4] an approach of mixers analysis in the frequency domain by the nodal equations method that allows a results representation in the generalized matrix form is developed. The analysis method is presented on the example of diode mixers. The developed method allows the presentation of results in a symbolic form and makes possible the procedure of optimal parametric synthesis of mixer circuits.

This paper is structured according to the following. In Section 2, the decomposition of the transistor current in a linear approximation is presented. A linear analysis of transistor mixers (balanced circuit, double balanced circuit and triple balanced circuit) including analysis of conversion gain, port isolation and mismatch effects is presented in Section 3. In Section 4, the parametric optimization approach is presented. The results of analytical calculations and simulations are presented in Section 5. Finally, Section 6 provides conclusions.

2. Current representation through a nonlinear element (transistor) in linear approximation

The diode-connected transistor is always in saturation mode. The current of the transistor in saturation mode can be represented as an expression:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(U_{GS} - V_{th})^2 ,$$

where L is transistor channel length, W is transistor gate width, μ is surface mobility, C_{ox} is oxide capacitance. The gate-to-source voltage U_{GS} is a function of the voltages applied to the mixer: $U_{GS} = f(U_0,\ U_{LO},\ U_{IF})$, U_0 is amplitude of the input signal at the carrier frequency ω_0, U_{LO} is the reference signal at the local oscillator frequency ω_{LO}, U_{IF} is amplitude of the output signal at the intermediate frequency ω_{IF}. Consider the initial phases of the signals at the carrier frequency, intermediate frequency and LO frequency are equal to zero, and the LO signal is harmonic. Then the considered signals take the form

$$U_0 = U_{0m}\cos\omega_0 t,\ U_{LO} = U_{LOm}\cos\omega_{LO} t,\ U_{IF} = U_{IFm}\cos\omega_{IF} t .$$

In the case of large LO amplitude approximation the following expressions are correct $U_{LOm} \gg U_{0m}$, $U_{LOm} \gg U_{IFm}$. Therefore, the gate-to-source voltage is equal to the LO voltage $U_{GS} \approx U_{LO}$ and transistor current is

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(U_{LO} - V_{th})^2 . \qquad (1)$$

Transconductance $g_m(U_{LO})$ is a function of the applied voltage and it can be represented as

$$g_m(U_{LO}) = \frac{\partial I_D}{\partial U_{LO}} = \mu C_{ox}\frac{W}{L}(U_{LO} - V_{th}) .$$

Generally, the voltage applied to the transistor gates can be represented as the sum of the AC and DC components of the LO voltage:

$$U_{LO} = U_{LO\sim} + U_{LO=} \, . \qquad (2)$$

Then the alternating component is represented as $U_{LO\sim} = U_{LOm} \cos \omega_{LO} t$, and the direct component $U_{LO=}$ is the bias voltage. The formula for the transconductance is

$$g_m(U_{LO}) = \frac{\partial I_D}{\partial U_{LO}} = \mu C_{ox} \frac{W}{L} (U_{LOm} \cos \omega_{LO} t + U_{LO=} - V_{th}) \, .$$

As was shown in [4], the current in the frequency domain follows the expression

$$I(p) = G_0 U_0(p_0) + 0.5 G_1 U_0(p_0 \pm j\omega_{LO}) + G_0 U_{IF}(p_0 \pm j\omega_{LO}) + \\ + G_1 U_{IFm}(p_0),$$

G_0 and G_1 are the coefficients of the $g_m(U_{LO})$ function Fourier series decomposition of cosine harmonics with frequency ω_{LO}. These coefficients are determined by the following expressions

$$G_0 = \mu C_{ox} \frac{W}{L} \left(\frac{2U_{LOm}}{\pi} + U_{LO=} - V_{th} \right) = \alpha \left(\frac{2U_{LOm}}{\pi} + U_{LO=} - V_{th} \right),$$

$$G_1 = \mu C_{ox} \frac{W}{L} \left(U_{LOm} + \frac{4(U_{LO=} - V_{th})}{\pi} \right) = \alpha \left(U_{LOm} + \frac{4(U_{LO=} - V_{th})}{\pi} \right),$$

where $\alpha = \mu C_{ox} \dfrac{W}{L}$.

3. Linear analysis of transistor mixers

In [4], an equivalent parametric circuit of the nonlinear element (Fig. 1) used in the further analysis was designed.

Diode-connected transistor equivalent parametric model includes four parallel connected elements. These elements are diode-connected transistor conductance G_0 , two VCCSs $0{,}5G_1U_0(p_0 \pm j\omega_{LO})$ and $G_1U_{IF}(p_0)$, and a current source I_0 that corresponds to the current of the local oscillator.

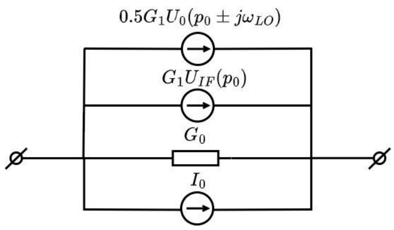

Fig. 1. Parametric transistor model

3.1. Conversion gain analysis and port isolation analysis

In [4], a generalized analysis approach for the diode frequency mixers (balanced circuit (B), double balanced circuit (DB) and triple balanced circuit (TB)) conversion gain and port isolation (RF-IF and LO-IF is presented. The developed approach is also used to analyze the conversion gain and port isolation of mixers using diode-connected transistors (Fig. 2).

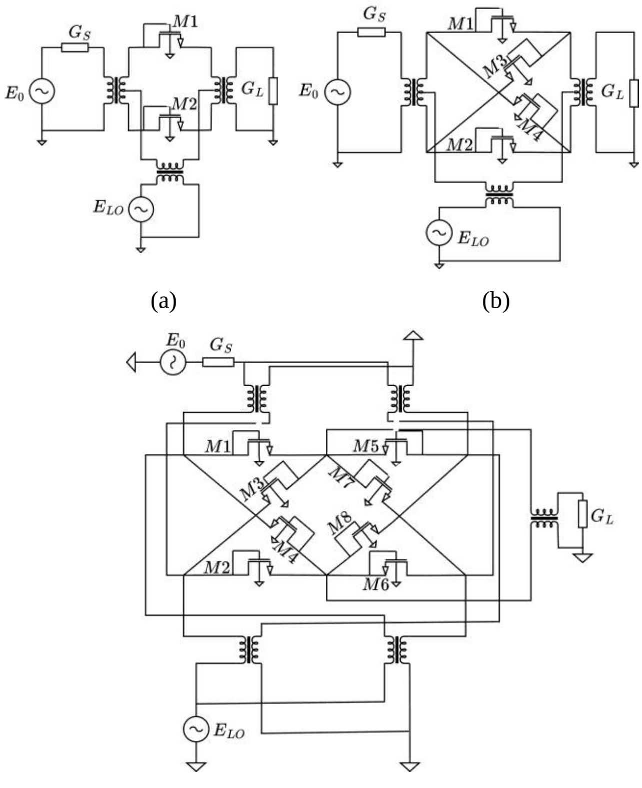

Fig. 2. Mixers using diode-connected transistors (a – balanced circuit, б – double balanced circuit, в – triple balanced circuit)

As an example, an analysis of conversion gain of the balanced mixer using diode-connected transistors is presented. The equivalent circuit of a balanced mixer is a balanced 4-pole in which there is no ground node. Therefore, the *Y*-matrix of such system is undefined, and the determinant of this matrix is equal to zero. In order to analyze such a circuit, the reference circuit is reduced to a symmetric form according to the Bartlett's bisection theorem. For this purpose, the input conductance G_S is separated into two elements with the value of $2G_S$, and the input source is represented as two grounded sources

$$E_0 = E_0^+ - E_0^- \, , \; E_0^+ = -E_0^- \, , \; \left| E_0^+ \right| = \left| E_0^- \right| = E_0 / 2 \, .$$

The mixer equivalent circuit for conversion gain analysis is shown in Fig. 3. Systems of nodal equations on the arguments p_0 (3) and $p_0 \pm j\omega_{LO}$ (4) in matrix form are presented.

$$\left[Y(p_0) \right] \begin{bmatrix} U_1(p_0) \\ U_2(p_0) \\ U_3(p_0) \\ U_4(p_0) \\ U_5(p_0) \\ U_6(p_0) \end{bmatrix} = \begin{bmatrix} 0.5GE_0 \\ -0.5GE_0 \\ 0.5G_{11}U_{01}(p_0 \pm j\omega_{LO}) \\ 0.5G_{12}U_{02}(p_0 \pm j\omega_{LO}) \\ -0.5G_{11}U_{01}(p_0 \pm j\omega_{LO}) \\ -0.5G_{12}U_{02}(p_0 \pm j\omega_{LO}) \end{bmatrix}, \qquad (3)$$

$$\left[Y(p_0 \pm j\omega_{LO})\right]\begin{bmatrix} U_1(p_0 \pm j\omega_{LO}) \\ U_2(p_0 \pm j\omega_{LO}) \\ U_3(p_0 \pm j\omega_{LO}) \\ U_4(p_0 \pm j\omega_{LO}) \\ U_5(p_0 \pm j\omega_{LO}) \\ U_6(p_0 \pm j\omega_{LO}) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ G_{11}U_{IF1}(p_0) \\ G_{12}U_{IF2}(p_0) \\ -G_{11}U_{IF1}(p_0) \\ -G_{12}U_{IF2}(p_0) \end{bmatrix}. \quad (4)$$

The voltages $U_{01}(p_0 \pm j\omega_{LO})$, $U_{02}(p_0 \pm j\omega_{LO})$, $U_{IF1}(p_0)$, $U_{IF2}(p_0)$ are expressed through the nodal potential as

$$U_{01}(p_0 \pm j\omega_{LO}) = U_5(p_0 \pm j\omega_{LO}) - U_3(p_0 \pm j\omega_{LO}),$$

$$U_{02}(p_0 \pm j\omega_{LO}) = U_6(p_0 \pm j\omega_{LO}) - U_4(p_0 \pm j\omega_{LO}),$$

$$U_{IF1}(p_0) = U_5(p_0) - U_3(p_0),\ U_{IF2}(p_0) = U_6(p_0) - U_4(p_0).$$

In the absence of reactance elements in mixer circuit, the *Y*-matrix is independent of frequency *Y*[p_0]=*Y*[$p_0 \pm j\omega_{LO}$]=[*Y*]. It is equal to

$$[Y] = \begin{bmatrix} G+2G_S & 0 & 0 & 0 & -2G_S & 0 \\ 0 & G+2G_S & 0 & 0 & 0 & -2G_S \\ 0 & 0 & G_{01}+G_L & -G_L & -G_{01} & 0 \\ 0 & 0 & -G_L & G_{02}+G_L & 0 & -G_{02} \\ -2G_S & 0 & -G_{01} & 0 & G_{01}+2G_S & 0 \\ 0 & -2G_S & 0 & -G_{02} & 0 & G_{02}+2G_S \end{bmatrix}.$$

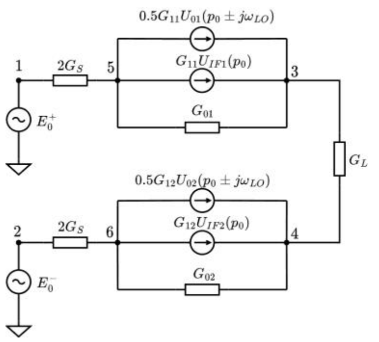

Fig. 3. Equivalent circuit of balanced mixer using diode-connected transistors for conversion gain analysis

The equations obtained in [4] are also valid for the calculation of the conversion gain and port isolation (RF-IF and LO-IF) of mixers using diode-connected transistors. These equations correspond to

$$K_B = \frac{4G_S^2 G_L G_1}{2(G_0(G_S+G_L)+2G_L G_S)^2 - G_1^2(G_S+G_L)^2},$$

$$K_{DB} = 2K_B,\ K_{TB} = 4K_B,$$

$$K_{\mathrm{B}\,RF-IF} = \frac{G_S(G_0 + G_1(1-K_B))}{(G_0+2G_L)G_S + G_0 G_L},$$

$$K_{\mathrm{DB}\,RF-IF} = 0,\ K_{\mathrm{TB}\,RF-IF} = 0,$$

$$K_{\mathrm{B}\,LO-IF} = 0,\ K_{\mathrm{DB}\,LO-IF} = 0,\ K_{\mathrm{TB}\,LO-IF} = 0.$$

3.2. Analysis of mismatch effects

The results presented earlier were obtained for the idealized case, i.e. there is no transistor parameters variation. However, in real circuits there is a mismatch effect of nonlinear element parameters, which directly influences the values of the conversion gain and port isolation. Usually, the parameters variation is about 20%.

During linear analysis [4], an approach to analyzing mismatch effects in diode mixers is developed. The obtained equations are also valid for estimating changes of conversion gain and port isolation due to mismatch effects in transistor mixers. For a balanced mixer, the following expressions determine the changes of conversion gain and RF-IF isolation and LO-IF isolation

$$\Delta K_B = \frac{2G_L G_S^2[2(G_0(G_S+G_L)+2G_L G_S)^2 + G_1^2(G_S+G_L)^2](\Delta G_{11}+\Delta G_{12})}{[2(G_0(G_S+G_L)+2G_L G_S)^2 - G_1^2(G_S+G_L)^2]^2} - \frac{8G_L G_S^2[G_0(G_S+G_L)^2 + 2G_L G_S(G_S+G_L)]G_1(\Delta G_{01}+\Delta G_{02})}{[2(G_0(G_S+G_L)+2G_L G_S)^2 - G_1^2(G_S+G_L)^2]^2},$$

$$\Delta K_{B\ RF-IF} = \frac{0.5G_S(1-K_B)(G_0(G_S+G_L)+2G_L G_S)(\Delta G_{11}+\Delta G_{12})}{(G_0(G_S+G_L)+2G_L G_S)^2} - \frac{(0.5G_1 G_S(1-K_B)(G_S+G_L) - G_L G_S^2)(\Delta G_{01}+\Delta G_{02})}{(G_0(G_S+G_L)+2G_L G_S)^2},$$

$$\Delta K_{B\ LO-IF} = -\frac{G_S G_{LO1}(\Delta G_{01} - \Delta G_{02})}{(G_0(G_S+G_L)+2G_S G_L)G_0}.$$

G_{LO1} is the LO source conductance and it is determined through the ratio of $\dfrac{I_{LO1}(p_{LO})}{U_{LOm}}$. $I_{LO1}(p_{LO})$ is defined as the first coefficient of the Fourier series

$$I_{LO1} = 2\frac{1}{T}\int_0^T I_D \cos\omega_{LO}t\,dt = \frac{2}{T}\int_0^T \frac{1}{2}\mu C_{ox}\frac{W}{L}(U_{LO}-V_{th})^2\cos\omega_{LO}t\,dt,$$

where $T = \dfrac{2\pi}{\omega_{LO}}$ is period of the LO frequency. Taking into account formula (2), the expression for $I_{LO1}(p_{LO})$ becomes as follows

$$I_{LO1} = \frac{2}{T}\int_0^T \frac{1}{2}\mu C_{ox}\frac{W}{L}(U_{LOm}\cos\omega_{LO}t + U_{LO=} - V_{th})^2\cos\omega_{LO}t\,dt = \mu C_{ox}\frac{W}{L}U_{LOm}(U_{LO=} - V_{th})$$

For a double balanced mixer these characteristics are defined as

$$\Delta K_{DB} = \{\{2G_L G_S^2[2(G_0(G_S+G_L)+2G_L G_S)^2 + G_1^2(G_S+G_L)^2](\Delta G_{11} + \Delta G_{12} + \Delta G_{13} + \Delta G_{14})\} - \{8G_L G_S^2[G_0(G_S+G_L)^2 + 2G_L G_S(G_S+G_L)]G_1(\Delta G_{01}+\Delta G_{02}+\Delta G_{03}+\Delta G_{04})\}\} / \{[2(G_0(G_S + G_L) + 2G_L G_S)^2 - G_1^2(G_S+G_L)^2]^2\},$$

$$\Delta K_{DB\ RF-IF} = \{\{0.5G_S(1-K_{DB})(G_0(G_S+G_L)+2G_LG_S)((\Delta G_{11}+\Delta G_{12})-$$
$$-(\Delta G_{13}+\Delta G_{14}))\}-\{(0.5G_1G_S(1-K_{DB})(G_S+G_L)-G_LG_S^2)((\Delta G_{01}+$$
$$+\Delta G_{02})-(\Delta G_{03}+\Delta G_{04}))\}\}/\{(G_0(G_S+G_L)+2G_LG_S)^2\},$$

$$\Delta K_{DB\ LO-IF} = -\frac{G_SG_{LO1}((\Delta G_{01}-\Delta G_{02})+(\Delta G_{03}-\Delta G_{04}))}{(G_0(G_S+G_L)+2G_SG_L)G_0},$$

and for the triple balanced circuit these characteristics are defined as

$$\Delta K_{TB} = \{\{2G_LG_S^2[2(G_0(G_S+G_L)+2G_LG_S)^2+G_1^2(G_S+G_L)^2](\Delta G_{11}+$$
$$+\Delta G_{12}+\Delta G_{13}+\Delta G_{14}+\Delta G_{15}+\Delta G_{16}+\Delta G_{17}+\Delta G_{18})\}-$$
$$-\{8G_LG_S^2[G_0(G_S+G_L)^2+2G_LG_S(G_S+G_L)]G_1(\Delta G_{01}+\Delta G_{02}+$$
$$+\Delta G_{03}+\Delta G_{04}+\Delta G_{05}+\Delta G_{06}+\Delta G_{07}+\Delta G_{08})\}\}/\{[2(G_0(G_S+$$
$$+G_L)+2G_LG_S)^2-G_1^2(G_S+G_L)^2]^2\},$$

$$\Delta K_{TB\ RF-IF} = \{\{0.5G_S(1-K_{TB})(G_0(G_S+G_L)+2G_LG_S)((\Delta G_{11}+$$
$$+\Delta G_{12})-(\Delta G_{13}+\Delta G_{14})+(\Delta G_{17}+\Delta G_{18})-(\Delta G_{15}+\Delta G_{16}))\}-$$
$$-\{(0.5G_1G_S(1-K_{TB})(G_S+G_L)-G_LG_S^2)((\Delta G_{01}+\Delta G_{02})-$$
$$-(\Delta G_{03}+\Delta G_{04})+(\Delta G_{07}+\Delta G_{08})-(\Delta G_{05}+\Delta G_{06}))\}\}/\{(G_0(G_S+$$
$$+G_L)+2G_LG_S)^2\},$$

$$\Delta K_{TB\ LO-IF} = -\{G_SG_{LO1}((\Delta G_{01}-\Delta G_{02})+(\Delta G_{03}-\Delta G_{04})+$$
$$+(\Delta G_{05}-\Delta G_{06})+(\Delta G_{07}-\Delta G_{08}))\}/\{(G_0(G_S+G_L)+2G_SG_L)G_0\}.$$

4. Mixer parametric optimization

In the recent years, in order to provide the advantages of telecommunication systems, it is necessary to use mixers with high quality operation in the high-frequency range. This requires the method development of optimal parametric synthesis techniques that allow the design of mixers with improved characteristics (maximum conversion gain and minimum of nonlinear distortion and noise figure).

In this paper the parametric optimization of three mixer circuits is considered. The parametrization is carried out according to the criteria of maximizing the conversion gain by choosing the optimal value of transistor gate width. The external mixer parameters such as bias voltage, LO voltage amplitude and load resistance are assumed to be specified.

The maximum of the balance mixer conversion gain is achieved at the value of the transistor gate width, which is the solution of the equation $\frac{\partial K_B}{\partial W} = 0$:

$$W = \frac{L}{\mu C_{ox}} \frac{4\pi G_L G_S}{(G_L+G_S)a}, \tag{5}$$

where

$$a = \sqrt{2(\pi^2-8)(2U_{LO=}-4U_{LO=}V_{th}+2V_{th}^2-U_{LOm}^2)},$$

the maximum of the conversion gain corresponds to

$$K_{Bm} = \frac{G_S}{(G_L+G_S)} \cdot \frac{(\pi U_{LOm}+4U_{LO=}-4V_{th})}{2((U_{LO=}-V_{th})\pi+2U_{LOm})+a}$$

For DB and TB frequency mixers, the maximum of conversion gain is determined by the similar way. For a DB mixer, the conversion gain maximum is equal to $K_{DBm} = 2K_{Bm}$, and for a TB mixer is equal to $K_{TBm} = 4K_{Bm}$. The optimal value of the transistor gate width for both circuits is calculated by formula (5).

5. Calculation and simulation

Calculation and modeling of mixers using diode-connected transistors were carried out. The mixers were simulated in Cadence using UMC 180 nm CMOS technology. For this PDK, the transistor threshold voltage is V_{th}=307.5 mV, and the range of transistor gate width is from 10 μm to 100 μm. The radio frequency (RF) that corresponds to ω_0 is 2.4 GHz, LO frequency is 2.5 GHz, U_{0m}=5 mV is the voltage amplitude of the signal at the carrier frequency, U_{LOm}=300 mV is the amplitude of the LO voltage, bias voltage $U_{LO=}$=600 mV, source resistance R_S and load resistance R_L correspond to the wave impedance and are equal to 50 Ω. The process parameters μC_{ox}, were determined from the *I-V* characteristics of the transistor. The value of the transistor channel length is 360 nm, as a double value of the minimum transistor channel length to reduce the influence of short-channel effects. The value of the transistor gate width is 50 μm as the average value of the gate width range. Table 1 shows the results of analytical calculation and simulation in Cadence Design Systems of the conversion gain and port isolation of three circuits (balanced mixer, double balanced mixer and triple balanced). The calculation and simulation results agree within 1 dB and confirm the high accuracy of the developed analysis method. In the Table 2 the results of calculation of errors introduced by mismatch effects are shown.

Table 1. Simulation and calculation results

		Circuit's type		
		B	DB	TB
K, dB	Calculation	–14.8	–8.8	–2.8
	Simulation	–14.4	–8.5	–3.1
K_{RF-IF}, dB	Calculation	–8.4	–	–
	Simulation	–7.9	–	–
K_{LO-IF}, dB	Calculation	–	–	–
	Simulation	–	–	–

The parametric optimization procedure showed that the maximum of the conversion gain is achieved when the transistor gate width is 66 μm. For a balanced mixer, the maximum of the conversion gain is –14.0 dB, for a double balanced mixer it is –7.9 dB, and for a triple balanced mixer it is –2.0 dB. Figure 4 shows the calculated and simulated dependence of the conversion gain on the transistor gate width for three mixer circuits. The dependencies have an extremum. The value of the transistor gate width, at which the maximum of the conversion gain is reached, corresponds to 60 μm. The maximum of the conversion gain of a balanced mixer is –14.1 dB, of a double balanced mixer is –8.1 dB, of a triple balanced mixer is –2.1 dB. It is also shown that by varying the transistor gate width over the range determined by PDK, the gain of the balanced mixer changes from –24 dB to –14 dB, the gain of the double balanced changes from –17 dB to –8 dB, and the gain of the triple balanced changes from –12 dB to –2 dB.

Table 2. Changes in three mixers characteristics due to mismatch effect

ΔD_1, %	ΔD_2, %	$\frac{\Delta K_B}{K_{B0}}$, %	$\frac{\Delta K_{B\,RF-IF}}{K_{B\,RF-IF0}}$, %	$\Delta K_{B\,LO-IF}$, dB
0	5	1.2	1.6	–45.4
0	7	1.6	2.2	–42.5
0	10	2.4	3.2	–39.4
ΔD_1, %	$\Delta D_{2\text{-}4}$, %	$\frac{\Delta K_{DB}}{K_{DB0}}$, %	$\frac{\Delta K_{DB\,RF-IF}}{K_{DB\,RF-IF0}}$, %	$\Delta K_{DB\,LO-IF}$, dB
0	5	3.5	1.6	–45.4
0	7	4.9	2.2	–42.5
0	10	7.0	3.2	–39.4
ΔD_1, ΔD_5, %	$\Delta D_{2\text{-}4,6\text{-}8}$, %	$\frac{\Delta K_{TB}}{K_{TB0}}$, %	$\frac{\Delta K_{TB\,RF-IF}}{K_{TB\,RF-IF0}}$, %	$\Delta K_{TB\,LO-IF}$, dB
0	5	7.1	1.6	–45.4
0	7	9.9	2.2	–42.5
0	10	14.1	3.2	–39.4

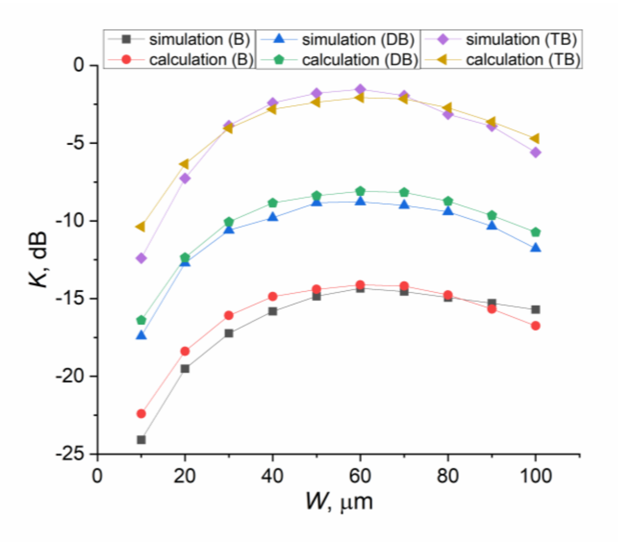

Fig. 4. Dependence of the conversion gain on the transistor gate width

5. Conclusions

The paper presents the analysis method of mixers using diode-connected transistors. The considered method allows the results to be represented in a symbolic form and the parametric optimization procedure of mixers. Linear analysis of three mixers (balanced circuit, double balanced circuit and triple balanced circuit) is considered, in particular the analysis of conversion gain, port isolation (RF-IF and LO-IF) and mismatch effects. A parametric optimization technique is developed for mixers using diode-connected transistors. Calculation and simulation were performed, difference between the results obtained analytically and the simulation results is within 1 dB. The results of the analysis of mixers using diode-connected transistors have shown that the highest conversion gain is found to occur with the triple balanced mixer, and the lowest conversion gain is observed for the balanced mixer. By varying the values of the transistor gate width it is possible to carry out the procedure of the mixer optimal synthesis and calculate the maximum value of the conversion gain.

The most important prospect of this work is the possibility of the formulation of conditions for optimal parametric synthesis of mixers: maximization of conversion gain, minimization of nonlinear distortion, minimization of intrinsic noise of mixers depending on circuit parameters, including internal parameters of active elements. The developed methods will allow the formation of expressions in symbolic form for estimation of the maximum achievable mixer characteristics, as well as synthesis of mixers with optimal parameters.

6. References

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