A New Single Switch Bridgeless SEPIC PFC Converter with Low Cost, Low THD and High PF

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Abstract

In this paper, a new single switch bridgeless AC/DC power factor correction PFC converter topology to achieve high PF and low THD is proposed. The proposed converter is based on the single ended primary inductance converter SEPIC topology. The SEPIC converters can operating from an input voltage that is greater or less than the output voltage. The proposed PFC uses only one active switch to PFC process together hoping higher PF and low THD. Besides the application cost is less than conventional bridgeless SEPIC PFC, in where two active switching devices are necessary. In order to verify the performance comparison between the proposed and the conventional SEPIC PFC, simulation circuit with 100W is install in PSIM. The simulation results are presented to demonstrate the feasibility of the proposed converters. The results show that the proposed bridgeless SEPIC PFC perfectly succeeds PFC operation using a single active switch.

1. Introduction

The request for developing power quality of the AC system has drawn excessive interest during the recent years. The increased usage of power electronic devices, such as variable speed drives, uncontrolled rectifiers and other switching devices, affects the power quality of the utility grid significantly. Standards similar to International Electro technical Commission (IEC) 61000-3-2 restrict the harmonics generated by these equipments [1]. To reduce harmonics in energy transmission lines, the research on active power factor correction (PFC) techniques has taken on an accelerated path [2-5].

Typical PFC converter topologies are boost [6,7], buck-boost [8], buck [9-11] and SEPIC [12-17]. The boost PFC converter is often used in practical applications, as the input current can be conveniently formed into a sinusoidal waveform to obtain unity power factor. However, the boost PFC converter has a restricted capability since the DC output voltage must be higher than the peak value of the AC input voltage [8]. On the other hand, the DC output voltage of the buck PFC is lower than the peak of the AC input voltage, which allows reducing components ratings and the cost. [11]. A buck PFC converter procures an alternative for low-voltage applications such as a 48V DC bus. Moreover, the buck PFC can obtain high efficiency over the entire input voltage range with distorted input current that comfortably passes the limits imposed by IEC 61000-3-2 requirements [1].

The input current of the buck PFC converter has dead zones along the cycle, which requires extensive passive filtering to improve the power factor. There is a tradeoff between output voltage choice and power factor. To solve this problem, SEPIC or Cuk converters were proposed. A conventional SEPIC converter can supply a high power factor in wide range of voltage conditions [13-14]. The conventional bridgeless SEPIC PFC converters involve two active switches to transmit an input current in keeping with the every cycle. This increases the application cost including the gate drivers and snubbers. Moreover, increasing the number of active switch equipments also decreases the reliability of the entire power stage.

This paper presents a new topology for single switch bridgeless AC/DC SEPIC PFC converters that reduces the THD and improves the PF of the operation with low cost. Proposed SEPIC converter combines the bridge and DC/DC stages into one stage and uses a single active switch. Therefore, the application cost can be decreased. Compared to the conventional bridgeless SEPIC PFC converter, the proposed converter uses two more diodes on the current path to avoid a short circuit condition, but reduce the number of the active switch whose realization cost is higher than several passive switching components such as a diode. So the total cost saving can be succeed. In the section 2, the proposed SEPIC converter topology and studying mode are analyzed in detail. In Section 3, the design procedure and control circuit of the proposed converter are explained. The power circuit model and simulation results of the proposed SEPIC converter are presented in Section 4. The conclusion is provided in Section 5.

2. Proposed Bridgeless SEPIC PFC Converter

In Fig. 1, a proposed bridgeless SEPIC PFC with one active switch is shown. Only one active switch Q_1 is used, and it transmits in an electrical cycle. When Q_1 turns on the entire cycle, the blocking diodes D_2 and D_3 are required to prevent confliction of positive and negative half cycles.

Fig 2 shows the operation of the proposed bridgeless SEPIC converter in a positive switching cycle. In fig. 2(a), V_s is positive and Q_1 is turned on. The input inductor current i_{L1} starts to rise linearly by a slope of V_{ac}/L_1. The voltage across L_2 is equal to the voltage of C_1 which follows the input voltage. Thus, i_{L2} decreases linearly by a slope of $-V_{ac}/L_2$. This mode ends by turning off Q_1. The input inductor current L_1 is written as follows:

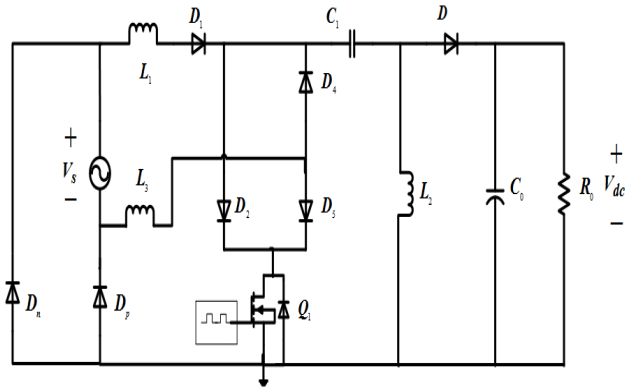


Fig. 1. Proposed bridgeless SEPIC PFC converter with single switch

$$i_s(t) = i_{L1}(t) = i_s(t_0) + V_{ac}(t_0)/L_1(t-t_0) \quad (1)$$

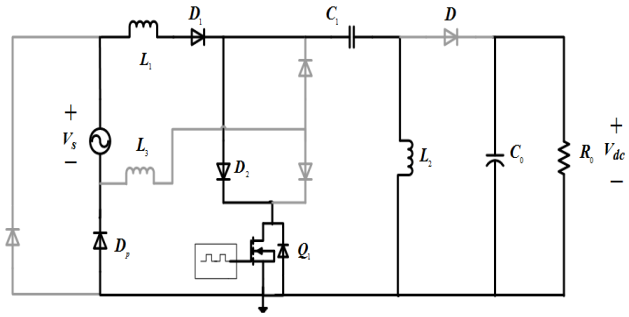
$$i_{L2} = i_s(t_0) - V_{ac}(t_0)/L_2(t-t_0) \quad (2)$$

In fig. 2(b), by turning Q_1 off, D begins to conduct. Input inductor current decreases linearly by a slope of $-V_0/L_1$, and i_{L2} increases linearly by a slope of V_0/L_2, i_{L2} is obtained as the following:

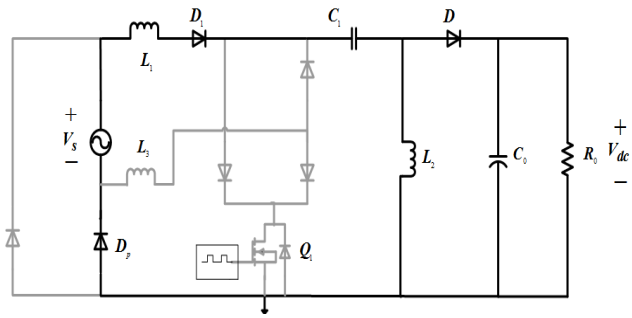
$$i_{L2}(t) = i_{L2}(t_1) + V_0/L_2(t-t_1) \quad (3)$$

In fig. 2(b), when D turns off, the current through inductors L_1 and L_2 are equal.

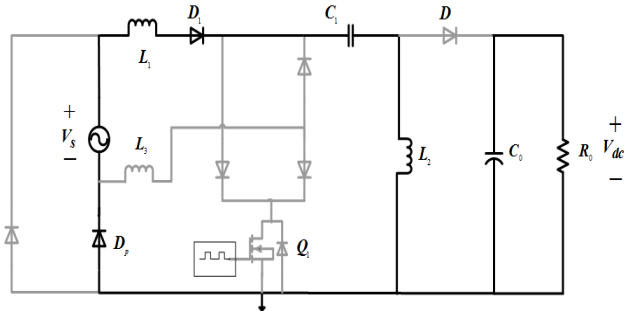
$$i_{L1} = i_{L2} \quad (4)$$



(a) when V_s is positive, Q_1 is turned on and D turn off



(b) when V_s is positive, Q_1 is turned off and D turn on



(c) when V_s is positive, Q_1 is turned off and D turn off

Fig 2. Operation of the proposed bridgeless SEPIC PFC converter in a positive switching cycle.

3. Design Procedure and Controller

3.1. Design Procedure

Following are the standard design equations of the main components of the AC/DC SEPIC PFC[15-17]. There are many factors involved in the design process of bridgeless SEPIC PFC. AC input voltage rms is 120V, DC output voltage is 48V, output power is 100W, input current peak is I_{in_peak}, input current ripple is $20\%I_{in\_peak}$, line frequency f_{ac} is 60 H_z and the switching operation frequency is f_s 30 kH_z. The following calculations are used to select the appropriate inductances for L_1 and L_2. If efficiency (η) is set equal to 95%, from the output power and converter efficiency, the following equation can be obtained:

$$I_{in\_peak} = I_1 = \frac{2\times P_0}{\eta \times V_1} = \frac{2\times 100}{0.95\times 120\times\sqrt{2}} = 1.24A$$
$$\Delta I_L = 20\% I_{in\_peak} = 0.25A \quad (5)$$

Input current ripple is

$$\Delta I_L = \frac{V_{ac}\times d}{L_1 \times f_s} \quad (6)$$

$$d \le \frac{V_0}{V_{ac}+V_0} \quad (7)$$

where d is the duty ratio. The output average current in a switching cycle can be obtained from Eq.8:

$$i_{DC\_avg} = \frac{i_{DC\_peak}\times d}{2} = \frac{V_{ac}^2(t_0)d^2T_s}{2L_eV_0} \quad (8)$$

where I_{DC_peak} is the peak current and it can be obtained from the following relation:

$$i_{DC\_peak} = i_{L1}(t_1) + i_{L2}(t_1) = \frac{1}{L_1} + \frac{1}{L_2}V_{ac}(t_0)dT_s \quad (9)$$

The average output current in one half of the line cycle can be obtained from Eq.10:

$$I_{DC\_avg} = \frac{1}{\pi}\int_0^{\pi} i_{DC\_avg}\, d\omega t = \frac{V_1^2 d^2 T_s}{4 L_e V_0} \quad (10)$$

thus from Eq. 7, d can be calculated as

$$d \le \frac{48}{120\times\sqrt{2}+48} \le 0.22 \quad (11)$$

selecting $d = 0.2$, L_e can be calculated from the following equation:

$$L_e = \frac{V_1^2 \times d^2}{4 \times V_0 \times f_s \times I_{0\_avg}} = \frac{(\sqrt{2}\times 120)^2 \times 0.2^2}{4\times 48\times 30000\times 1.17} = 237\mu H \quad (12)$$

L_1 can be calculated as

$$L_1 = \frac{V_1 \times d}{f_s \times \Delta I_L} = \frac{\sqrt{2}\times 120\times 0.2}{30000\times 0.25} = 4.4mH \quad (13)$$

Therefore, L_2 can be calculated from the following equation

$$\frac{1}{L_2} = \frac{1}{L_e} - \frac{1}{L_1} = \frac{1}{237\mu H} - \frac{1}{4.4mH} \Rightarrow L_2 = 100\mu H \quad (14)$$

The output capacitance required to achieve a desired percentage bus ripple can be expressed as :

$$C_0 = \frac{P_{load}}{V_{out}\times \Delta V_{bus(\%)} \times 4 \times f_{ac}} = \frac{100}{48\times 5\times 4\times 60} = 2.1mF \cong 2200\mu F \quad (15)$$

3.2. Control Circuit

Fig. 3 shows the block diagram of the control circuit. The control circuit consists of one voltage control loop and one current control loop. Two proportional integral PI controllers are used for each control loop.

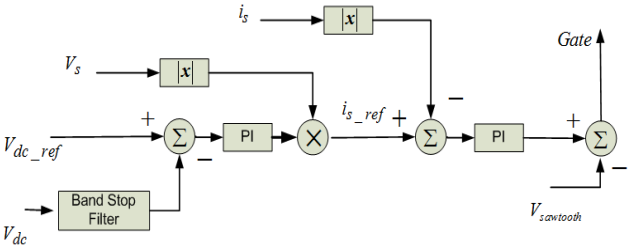


Fig. 3. Block diagram of controller

The high frequency switching of the inverter causes switching ripples on the DC bus. These switching ripples can introduce an error in reference signal estimation. Therefore the sensed DC link voltage is processed by using a band stop filter BSF before comparison with the reference value. By doing so, the dynamic property of the voltage control loop can be developed without introducing unnecessary 120Hz component in the current reference.

4. Simulation Results

The parameters of the power circuits for all SEPIC PFC are summarized in Table 1. The proposed bridgeless SEPIC topology is simulated to compare with conventional SEPIC. PSIM simulation software was used to verify the steady state waveforms of each component. The duty ratio reference was selected as 0.2 which corresponds the required duty reference to produce 48V output at the peak of the input voltage. The 2nd order band stop filter gain, center frequency and stopping band are designed as 1, 120 and 20, respectively.

Table 1. The parameters for the simulation circuit

Input inductances L_1	4.4 mH
Output capacitance C_o	2100 µF
Voltage input capacitance C_1	1 µF
Output inductances L_2	100µH
Input voltage V_{rms}	120 V
Rated output power P_o	100 W
Output voltage reference V_{ref}	48 V
Operating frequency f_{ac}	60 Hz
Switching frequency f_s	30 kHz

4.1. PSIM Simulation of Conventional SEPIC PFC Converter

Fig. 4 shows the switching model for simulation circuit of conventional SEPIC PFC in PSIM. In the switching model, all active and passive switching devices are assumed as ideal elements, so their voltage drops are ignored.

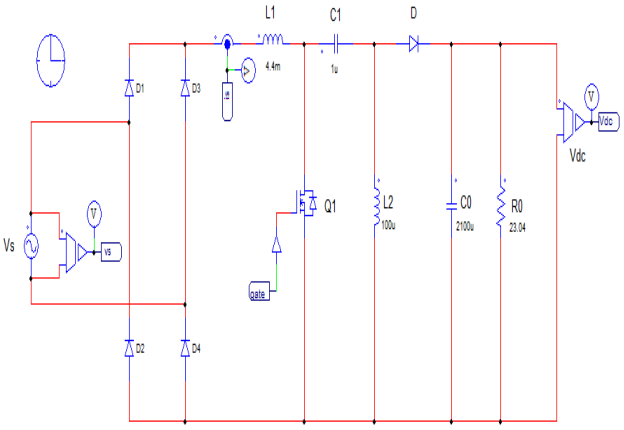


Fig. 4. PSIM simulation circuit for conventional SEPIC PFC

Fig. 5 shows input current and output voltage signals for conventional SEPIC PFC. As shown in the fig.5, the input current is regulated sinusoidally and the output voltage is controlled to 48V. In the output voltage, the well known double frequency ripple, here 120Hz. Fig. 6 shows transient signals for conventional SEPIC PFC. The PF and THD values are measured as respectively 0.994 and 7.47%.

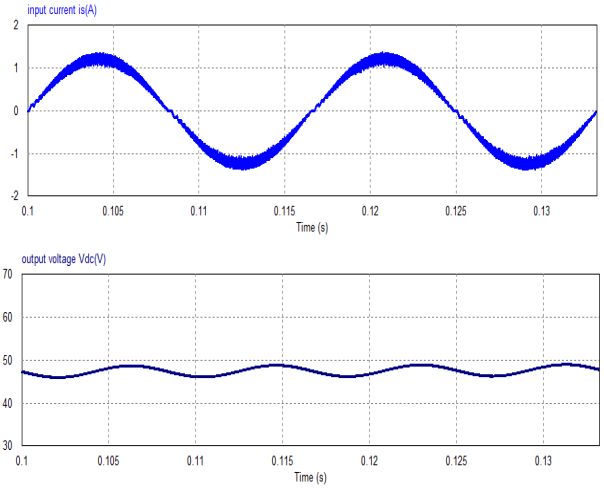


Fig. 5. Input current and output voltage for conventional SEPIC

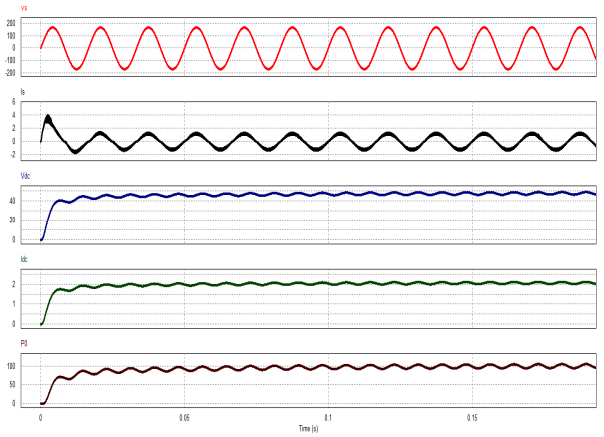


Fig. 6. The transient signals for conventional SEPIC PFC

4.2. PSIM Simulation of Proposed Bridgeless SEPIC PFC Converter

Fig. 7 shows the switching model for simulation circuit of proposed bridgeless SEPIC PFC converter in PSIM. In the switching model, all active and passive switching devices are assumed as ideal elements, so their voltage drops are ignored.

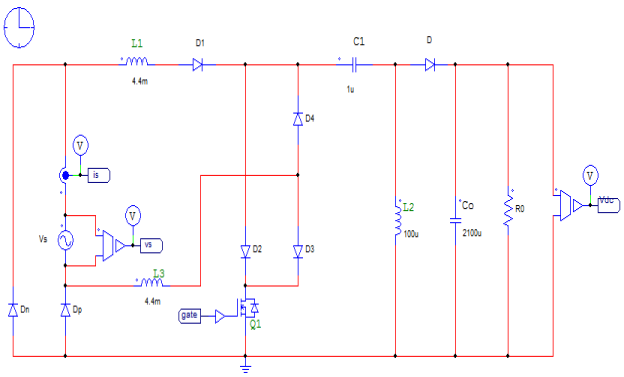


Fig. 7. PSIM simulation circuit for proposed bridgeless SEPIC PFC

Fig. 8 shows input current and output voltage signals for proposed bridgeless SEPIC PFC. As shown in the fig.8, the input current is regulated sinusoidally and the output voltage is controlled to 48V. In the output voltage, the well known double frequency ripple, here 120Hz. Fig. 9 shows transient signals for proposed bridgeless SEPIC PFC. The PF and THD values are measured as respectively 0.998 and 4.88%.

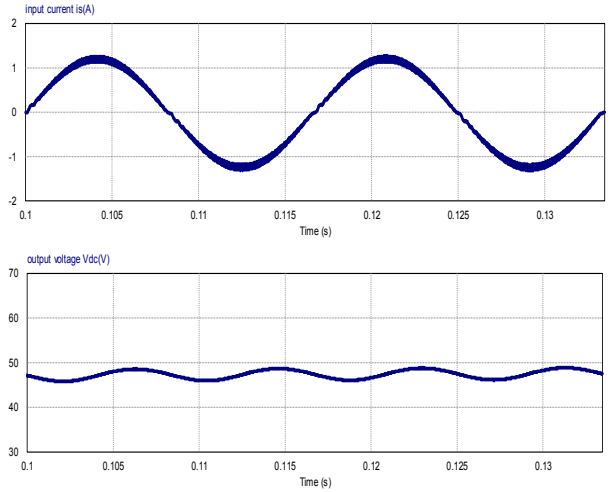


Fig. 8. Input current and output voltage for proposed bridgeless SEPIC PFC

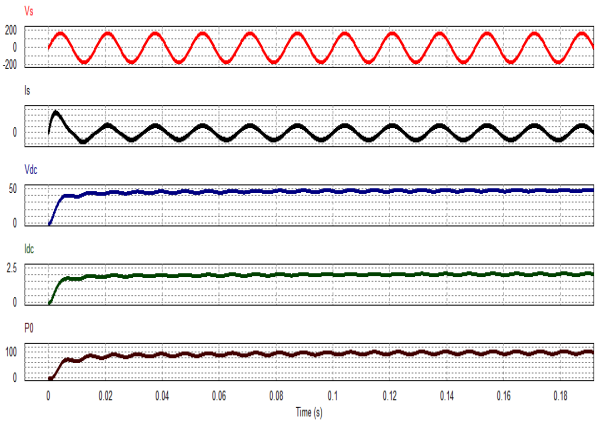


Fig. 9. The transient signals for proposed bridgeless SEPIC PFC

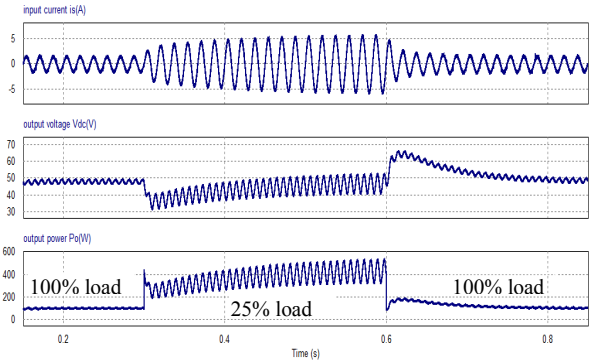


Fig. 10. The transient response of the proposed SEPIC PFC simulation model

The transient response of the improved simulation model are shown in Fig10. The load is adjusted at t=0.3s from 100 percent to 25 percent in step in the simulation. As shown in the Fig 10, the input current and the output voltage controls are stable and the voltage is very well regulated. At t=0.6s, the load is adjusted to 100 percent. In that condition, there is no significant transient problem. DC output voltage is 48V. It can be observed from this figure that input current is in phase with input voltage and is practically sinusoidal with low total harmonic distortion and high power factor, output voltage which is regulated at around 48V, with a 120 H_z low frequency ripple.

Conventional and bridgeless SEPIC PFC converters are compared in Table 2. The PF and THD values for proposed converter are measured as respectively 0.998 and 4.88%. The simulations show that it is an excellent option for proposed bridgeless SEPIC PFC with single active switch for lower power applications.

Table 2. Compare of SEPIC PFCs in terms of THD and PF

	THD(%)	PF
Conventional SEPIC PFC	7.47 %	0.994
Proposed bridgeless SEPIC PFC with one active switch	**4.88%**	**0.998**

5. Conclusion

In this paper, a single phase bridgeless SEPIC PFC converter topology with single active switch has been proposed. For the proposed converter, the circuit topology, the operation modes, design procedure and the control circuit have been shown in detail. In order to see the performance of the proposed SEPIC converter, a 100W switching model was built in PSIM software package. The total harmonics distortion and power factor were calculated by using THD tool and PF tool. Comparisons were made between the proposed bridgeless SEPIC converter and the conventional SEPIC converter. By using the improved simulation model, both the transient and the steady state operations have been investigated. The power factor and the source current total harmonic distortion are improved as 0.998 and 4.88% respectively. The simulation results shows a high input power factor, low total harmonic distortion. Since the proposed SEPIC converter uses only one single active switch, it is expected that the application cost can be decreased and the reliability of the entire power stage can be developed. It is an excellent option for single phase bridgeless SEPIC PFC topology solution for lower power equipments especially those requiring high quality and low THD input power.

6. Acknowledgment

This study is supported by the TUBITAK (The Scientific and Technological research Council of Turkey).

7. References

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