Broadband Transimpedance Amplifier TIA in CMOS 0.18µm Technology Using Matching Technique

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Abstract — **This paper describes the matching technique to improve the bandwidth of multi-GHz frequency ranges for the transimpedance amplifier (TIA). Different topologies can be used to implement the input matching network. It is shown that by simultaneously using of series input matching topology and T-output matching network, the bandwidth of the TIA can be obviously improved. This methodology is supported by a design example in a 0.18µm CMOS technology. Cadence tools simulation results show a -3dB bandwidth of 20GHz with 50fF photodiode capacitance, a transimpedance gain of 52.6dBΩ, 8.7p $/\sqrt{H}$ input referred noise and group delay less than 3ps. The TIA dissipates 1.3mW from a 1.8V supply voltage.**

Index Terms— Transimpedance amplifier (TIA), photodiode, matching network, input-referred noise and bandwidth extension.

I. INTRODUCTION

The continuous growth in the commercial wireless telecommunications market has been driving to satisfy the demands of high speed, low cost and high integration of radio-frequency (RF) broadband receivers [1]. Recently, it is reported that, every ten years, the speed of analog CMOS circuits increases by one order of magnitude. Moreover the performance of CMOS process is improving continually and reliably, due to the scaling down therefore it dominates the most expensive technologies [2].

One of the main challenges in receiver system is the design of a wideband transimpedance amplifier (TIA). Several circuits with different topologies have been reported for TIA. In CMOS technology, common source (CS) and common gate (CG) are the most used transistor configurations in TIA topologies. CS TIA has high gain and superior good noise performance. Inductive source degenerated is created by adding an inductor in the source of a CS stage. This technique improves both the gain and noise performance of TIA [3]. CG configuration provides a stable circuit with low power, less parasitic, and less noise performance [4].

The input matching mechanism is conceivable for CG configuration so that it is extensively used in wideband TIA circuits [5, 6]. On the other hand, CS configuration may be used in wideband TIAs using feedback network or matching circuits. Inductive source degenerated is usually used for CS configuration in narrowband TIA applications.

Cascode stage is generally used in CMOS RF circuits. It composes of a CS stage followed by a CG stage. Cascode configuration provides high power gain, better noise performance and low power consumption [7]. For low frequencies, the noise sources of the upper transistor is degenerated by the output impedance of the lower transistor [8]. Therefore, cascode stage configuration has better noise performance. In high frequencies, the admittance parasitic of common node (drain-source) increases as frequency increases. As a result, when the source impedance of upper transistor is low, its drain noise occuring at the output [4]. It is possible to improve the bandwidth of cascode stage using feedback techniques [9]. Matching networks in the input is another technique to enhance the bandwidth of cascode configuration [10].

The most significant characteristics of the TIA are transimpedance gain and noise performance. In additional to these characteristics, the important parameters in the design of transimpedance amplifier are bandwidth, power consumption and chip area. The minimum noise of the TIA can be achieved by using optimum noise matching. The maximum gain can be obtained by using conjugate impedance matching.

Since these two matching conditions are inconsistent, therefore both of maximum gain and minimum noise do not occur at the same time. The advantage of CMOS circuits is that, both noise and gain matching conditions are very close. This can improve the noise performance of CMOS TIA topologies. It is reported that simultaneous noise and power matching becomes possible in CMOS technology [11].

The study presented here applies a matching technique to improve the bandwidth of the transimpedance amplifier. It is based on using cascode topology. In the case of cascode topology, the input impedance is pure capacitive (in very low frequencies) so that a resistive part must be added to the input impedance. This can be done by connecting a degenerating inductance in the source of CS transistor or using a resistive feedback, or a parallel resistance in the gate. Source degenerated cascode or CS stage shows a good narrowband matching, high stability and good noise performance. By using resistive feedback or proper LC matching networks, both cascode and CS stages can be used in large bandwidth applications. On the other hand, CG configuration offers

wideband matching possibility. Applying proper matching networks at the input and the output nodes are the strategic phases in improving the bandwidth of the TIA.

This paper is organized as follows: Section II domenstrates the proposed TIA design. The matching technique to improve bandwidth is presented in section III and section IV. To demonstrate the practicality of this technique, the simulation results of a design example is followed in Section V.

II. THE PROPOSED TIA DESIGN

Arrangement of CS and cascode stage is beneficial in TIA design. It has been explored that combination of CS configuration in the first stage and cascode configuration in the second stage provides good noise performance of CS stage and high gain of cascode stage [12]. The noise is small because of capacitances and parasitic admittances existence at the cascode node. Moreover high gain and outstanding reverse isolation can be achieved. Although, two stage TIA consumes high power but it provides better gain. So that, the best topology of the proposed TIA design is cascading stages of CS cascode configuration as shown in Fig.1. Output matching is implemented using standard T network and the input matching technique will be explained in the next section.

III. INPUT MATCHING ANALYSIS

There are different topologies which could be used to implement the input matching. Probably the simplest matching network is using a series inductor at the gate of the input transistor as shown in Fig.1.

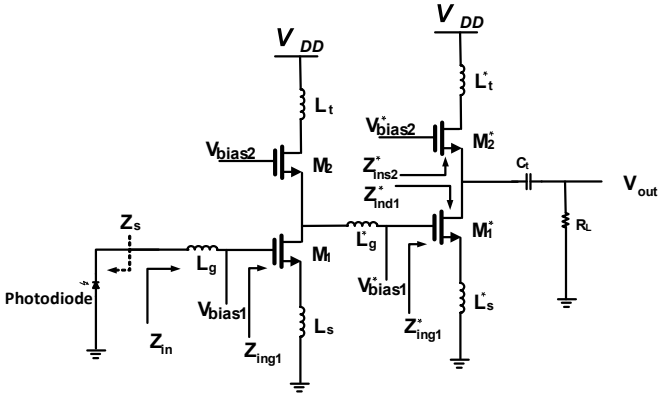

Fig. 1. Schematic of proposed TIA with series inductor as input matching network

Fig. 2 shows the small signal model of the input matching circuit of Fig.1. Neglecting the effect of the feedback capacitance $C_{g\ 1}$ of the input transistor M_1 and the drain-source conductance g_{o1} , the input impedance $Z_{i1\ \ 1}$ is given by :

$$Z_{\text{ing1}} = \frac{1}{\omega^2 L_s C_{gs1} g_{m1}} \cdot \frac{1}{1 + \dfrac{j\omega C_{gs1}}{\omega^2 L_s C_{gs1} g_{m1}}} \qquad (1)$$

where L_S is the degeneration inductor at the source of M_1 and g_{m1} is the transcondcutance of transistor M_1.

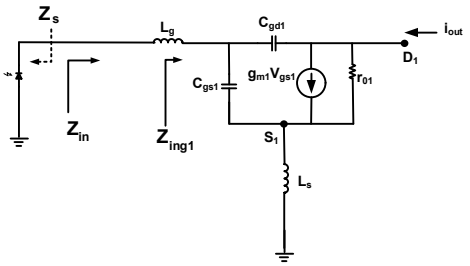

Fig. 2. Small signal model of the input side of Fig. 1.

The input impedance $Z_{i1\ \ 1}$ can be represented as the parallel of a resistance R_p with the capacitor C_g . Thus, the small signal model to calculate the input impedance Z_{i1} has to be redrawn as shown in Fig. 3.

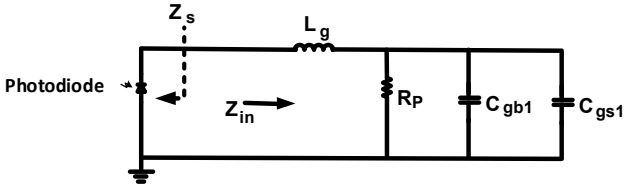

Fig. 3. Simplified small signal model to calculate of Z_{i1}

Now, the accurate expression to calculate the input impedance is given by:

$$Z_{in} = \frac{R_p}{1+\omega^2 R_p^2 C_T^2} + j\omega\left[\frac{L_g - R_p^2 C_T\left(1-\omega^2 L_g C_T\right)}{1+\omega^2 R_p^2 C_T^2}\right] \qquad (2)$$

where R_p and C_T are given by:

$$R_p = \frac{1}{\omega^2 L_s C_{gs1} g_{m1}}$$
$$C_T = C_{gs1} + C_{gb} \qquad (3)$$

In order to realize a conjugate matching of the transimpdance amplifier, the real part of $R\ \{Z_{i1}\}$ must be eaual the source resistance R_S and the imaginary compenent of $I_1\ \{Z_{i1}\}$ have to be complex conjugate of photodiode impedance X_S. That means:

$$R_s = \frac{R_p}{1+\omega^2 R_p^2 C_T^2},$$
$$-\omega\left[\frac{L_g - R_p^2 C_T\left(1-\omega^2 L_g C_T\right)}{1+\omega^2 R_p^2 C_T^2}\right] = \frac{1}{\omega C_{pd}} \qquad (4)$$

where C_p is the photodiode capacitance .

From eq.4 , we see that the matching conductions are satisfied by using the proper value of the inductances L_S and L_g.

Supposing that $\omega^2 R_p^2 C_T^2 \gg 1$, then $L_S$can be given by:

$$L_s = \frac{R_s}{\omega_T}\left(\frac{C_T}{C_{gs1}}\right) \qquad (5)$$

where ω_T is cut- off frequency and the approximated value of L_g is determined by :

$$L_g = \frac{1/C_{pd} + 1/C_{gs1}}{\omega R_s g_{m1}^2} \quad (6)$$

IV. OUTPUT MATCHING ANALYSIS

As shown in Fig. 4, we choose the T configuration for implement the output matching. In order to calculate the output impedance Z_o , first of all we have to determine the input impedance $Z_{in\ 2}^*$ of the drain of M_2^*.

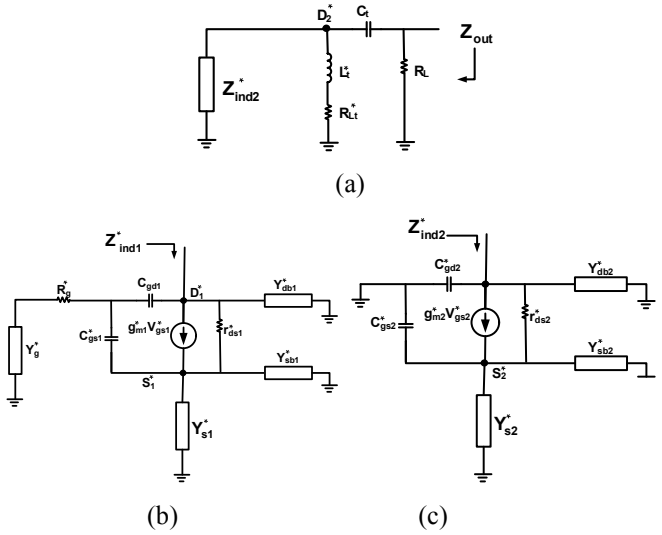

Fig. 4. (a) The output matching network (b) the small signal model to calculate the input impedance to the drain of M_1^* and M_2^*.

From the small signal circuit shown in Fig. 4(b), we have:

$$Y_{ind2}^* = Y_{db2}^* - \frac{\left(g_{m2}^* + g_{o2}^*\right)\left(C_{gs2}^* g_{o2}^* + C_{gd2}^* Y_{ss2}^*\right)}{Y_{ss2}^* C_{gs2}^*} + \left(j\omega C_{gd2}^* + g_{o2}^*\right) + \left(g_{m2}^* + g_{o2}^*\right)\frac{C_{gd2}^*}{C_{gs2}^*} \quad (7)$$

where $Y_{ss2}^* = Y_{s2}^* + Y_{sb2}^* + j\omega C_{gs2}^* + g_{m2}^* + g_{o2}^*$

Y_{s2}^* is the load at the source of transistor M_2^*, that given by ($Y_{s2}^* = Y_b^* + Y_{in\ 1}^*$) , where Y_b^* is substrate admittance of M_2^* and $Y_{in\ 1}^*$ is the input admittance to the drain of M_1^* .

$$Y_{ind1}^* = Y_{db1}^* + \frac{j\omega\left(C_{gs1}^* g_{ro1}^* + C_{gd1}^* y_{ss1}^*\right)}{j\omega C_{gs1}^*\left(-j\omega C_{gs1}^* - g_{m1}^*\right) + y_{ss1}^* y_{gg1}^*}\left(-j\omega C_{gd1}^* + g_{m1}^* - \frac{\left(g_{m1}^* + g_{ro1}^*\right)y_{gg1}^*}{j\omega C_{gs1}^*}\right) + \left(j\omega C_{gd1}^* + g_{ro1}^*\right) + \left(g_{m1}^* + g_{ro1}^*\right) \quad (8)$$

where $Y_{ss1}^* = Y_{s1}^* + Y_{sb1}^* + j\omega C_{gs1}^* + g_{m1}^* + g_{ro1}^*$ and

$$y_{gg1}^* = \frac{Y_{g1}^*}{1 + R_g^* Y_{g1}^*} + j\omega C_{gd1}^* + j\omega C_{gs1}^* .$$

Y_{g1}^* is the input admittance at the gate transistor M_1^*, and Y_{s1}^* is the load at the source of M_1^* which is given by : $Y_{s1}^* = Y_b^* +$ the admittance at the source of M_1^*.

$$Z_{out} = \frac{1}{j\omega C_t} + \omega L_t \frac{Q_t + \omega L_t G_{in2}^*\left(Q_t^{\ 2}+1\right) + j\left(Q_t^{\ 2} - \omega L_t B_{ind2}^*\left(Q_t^{\ 2}+1\right)\right)}{Q_t^{\ 2} + 2Q_t\omega L_t\left(G_{ind2}^* - Q_t B_{ind2}^*\right) + \omega^2 L_t^{\ 2}\left(Q_t^{\ 2}+1\right)\left(G_{ind2}^{*\ 2} + B_{ind2}^{*\ 2}\right)}$$

(9) where Q_t is the quality factor of L_t.

To satisify the complex conjugate matching conductions , the values of $R_{l\iota}$ and $X_{l\iota}$ are given by :

$$R_{load} = \omega L_t \frac{Q_t + \omega L_t G_{ind2}^*\left(Q_t^{\ 2}+1\right)}{Q_t^{\ 2} + 2Q_t\omega L_t\left(G_{ind2}^* - Q_t B_{ind2}^*\right) + \omega^2 L_t^{\ 2}\left(Q_t^{\ 2}+1\right)\left(G_{ind2}^{*\ 2} + B_{ind2}^{*\ 2}\right)} \quad (10)$$

$$X_{load} = \frac{1}{\omega C_t} = \omega L_t \frac{\left(Q_t^{\ 2} - \omega L_m B_{ind2}^*\left(Q_t^{\ 2}+1\right)\right)}{Q_t^{\ 2} + 2Q_t\omega L_t\left(G_{ind2}^* - Q_t B_{ind2}^*\right) + \omega^2 L_t^{\ 2}\left(Q_t^{\ 2}+1\right)\left(G_{ind2}^{*\ 2} + B_{ind2}^{*\ 2}\right)}$$

V. DESIGN EXAMPLE AND SIMULATION RESULTS

To demonstrate the effectiveness of the matching methodology, a design example was implemented using 0.18µm HV CMOS process. The cadence schematic editor and virtuoso editor are used to design and simulate our proposed example using RF transistor model. Simulations are done with a single supply (i.e.1.8V) and the presence of a 50fF photodiode capacitance. As shown in in Fig. 5, the frequency response of the provides a transimpdance gain of 53.7dB.Ω and bandwidth range of 1Khz -15GHz for schematic circuit and 20GHz bandwidth with 52.6dB.Ω transimpedance gain for the extracted TIA. The power consumption is in the range of 1.3mW.

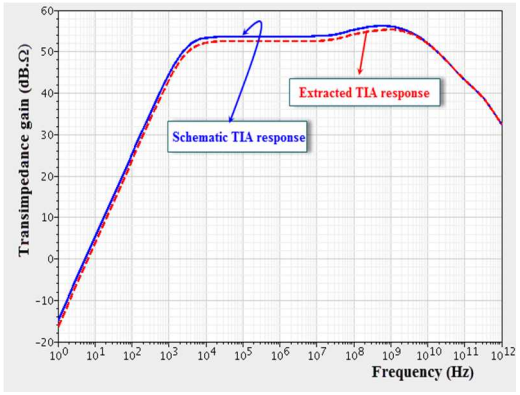

Fig. 5. The frequency response for C_p =50fF.

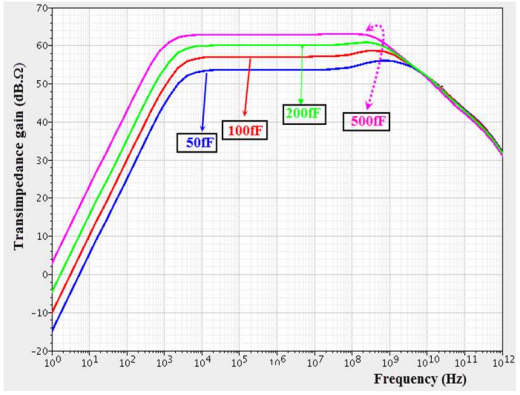

Fig. 6. The frequency response for different values of C_p

Fig. 6 shows the frequency response against the input capacitance C_p . For the photodiode capacitance of 100fF , the gain is 57dB.Ω and bandwidth is 4.5GHz and it is above 2GHz for C_p =200fF with gain of 60dB.Ω. For large value of photodiode capacitance 500fF, the gain becomes 63dB.Ω and 1GHz bandwith .

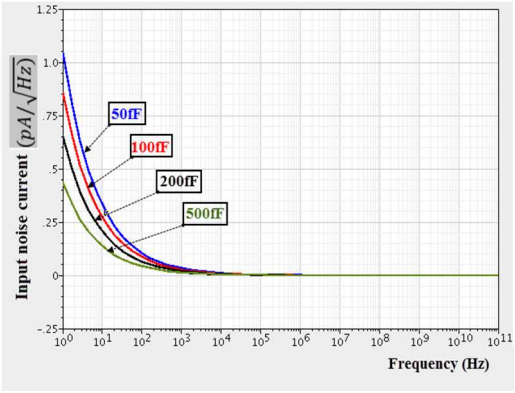

Fig. 7. The input noise current spectral density against the photodiode capacitance C_p .

The simulation of input noise current spectral density agianst the input capacitance C_p is depicted in Fig. 7. It shows that the noise is maximum at low frequencies then it falls and tends to zero at high frequencies over the desired bandwidth. The average input noise of the TIA is 8.7pA/$\sqrt{H}$ for input capacitance C_p =50fF and 8.7pA/$\sqrt{H}$ when C_p =500fF.

The group-delay variation is a significant parameter of TIA. Even with large enough bandwidth, distortions of the output may take place if the phase linearity of the TIA is insufficient. It can be observed in Fig. 8, within the bandwidth of 20 GHz, the TIA circuit has a group variation of less than 7ps .

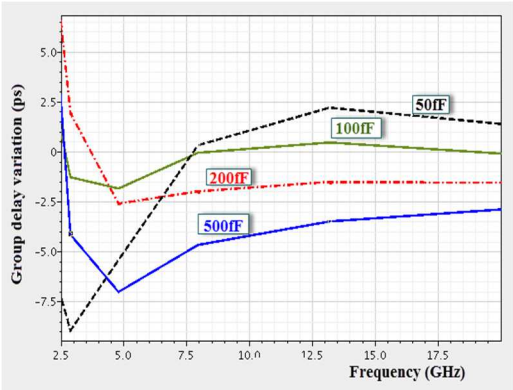

Fig. 8. Group delay variation of the TIA

Using series inductor at the gate on the input transistor has some drawbacks such as the value of the degeration inductor must be small to evade the gain drecrement. Another issues of using the serier inductor is not convenient for transmission line inductors. So that it is better to use this technique in short end to reduce the parasitic effects and to shorten the design process.

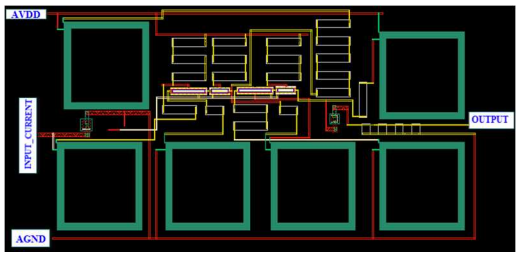

Fig. 9. Layout of the TIA

VI. CONCLUSION

This work demonstrates the performance of a transimpedance amplifier (TIA) using matching networks technique with cascode configuration. The proposed circuit and design methodlogy resolve a number of issues and provide wide bandwidth and low noise. The TIA is implemented in a 0.18µm CMOS technology. The cadence simulation results of the extracted circuit shows that the proposed TIA achives 20GHz -3dB bandwidth, 52.6dB.Ω transimpedance gain, 8.7pA/$\sqrt{H}$ input referred noise and a group variation of less than 7ps within the pass band. The power dissipation is 1.3mW from a 1.8V supply voltage.

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