A New VDTA Based Frequency Agile Filter

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Abstract

In this study, a new voltage mode frequency agile filter designed by voltage differencing trans-conductance amplifier (VDTA) is presented. A single VDTA and two capacitors are used to implement the designed frequency agile filter. The MOS capacitor technique is used instead of conventional capacitors to achieve high operating frequencies. The agility of the designed filter is implemented by selecting different size MOS capacitor. The performance parameters of the VDTA and agile filter structure are summarized. The suitability of the filter for different applications are given. AMS 0.18µm parameters are used for the designed frequency agile filter.

Keywords—Frequency agile filter, VDTA, Voltage-mode circuits, MOS capacitor

1. Introduction

Analog signal processing is essential part of telecommunications. Transceivers play key role in telecommunication. Mixing, filtering, amplifying, etc. are the main tasks of transceivers. Also, analog parts of the military and biomedical applications have great importance.

New trend of analog circuit design has been focused on reconfigurable analog elements for a long time. Especially, frequency hopped receivers need the reconfigurable band pass filter for encoding secret information. HAVEQUICK [1], Single Channel Ground and Airborne Radio System (SINCGARS) [2] are some example of hopping systems.

There are lots of technique to design reconfigurable filter. Some example of reconfigurable band pass filter (frequency agile filter) has been designed by BiCMOS transistors by the aid of CCCII [3, 4].

In this work, a new frequency agile filter is designed by voltage differencing trans-conductance amplifier. The agility is realized by selecting different capacitance digitally. MOS capacitor technique [5] are used instead of conventional capacitance technique for easy implementation. Also, MOS capacitor is preferred to increase the operating frequency of the designed frequency agile filter.

The organization of the paper is as follows. In second section the CMOS realization and layout of the VDTA is given. The classical floating current source [6] designed by Arbel and Goldminz are cascaded to construct the CMOS implementation of the voltage differencing trans-conductance amplifier. The performance of the filter are verified by the post layout simulations.

In third section the frequency agile filter structure is presented. The comparison with some conventional frequency agile filter are done for the designed filter.

2. CMOS realization of VDTA

VDTA is an analog signal processing building block which has two different trans-conductance values. Also these two trans-conductance values are electronically controllable by external biasing current. VDTA driven biquadratic filters, oscillators and FDNR (frequency dependent negative resistor) can be easily realized with only one VDTA block by the aid of these two different trans-conductance values.

VDTA has five terminals. All terminals exhibits high impedance values. Two of them are differential input voltage (V_P, V_N). The differential input is transferred to the current at the terminal Z output terminal by first trans- conductance gain. Then, the voltage drop at the terminal Z is transferred to current at the terminals X+ and X- by second trans-conductance gain [7].

The circuit description of the VDTA is given in Equation 1. The symbol of the voltage differencing trans-conductance amplifier is given in Fig.1.

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (1)$$

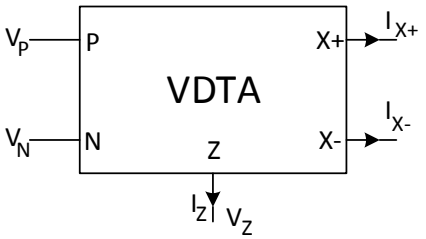

Fig. 1. VDTA block diagram

The CMOS realization of the VDTA can be implemented by using two floating current source proposed by Arbel and Goldminz [6]. The CMOS realization of the voltage differencing trans-conductance amplifier is given in Fig. 2. The floating current source has very simple implementation to operate high frequency range. The trans-conductance realization is available only four transistors.

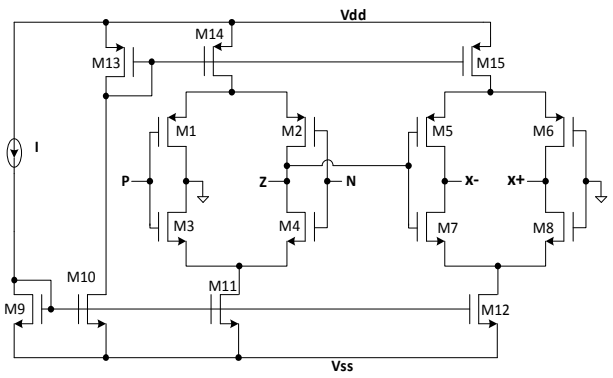

Fig. 2. CMOS realization of VDTA.

The transistor sizes of the voltage differencing trans-conductance amplifier are given in Table 1. M1, M2, M3 and M4 transistors belong to first floating current source. M5, M6, M7 and M8 transistors belong to second floating current source. The other transistors are used for biasing currents. The bias current is arranged as 115µA. The biasing circuit instead of I current is implemented basically as in Fig. 3.

Table 1. The size of the transistors

Transistors	Value
M_1, M_2, M_5, M_6	60u/0.36u
M_3, M_4, M_7, M_8	10u/0.36u
M_9, M_{10}, M_{11}, M_{12}	20u/1u
M_{13}, M_{14}, M_{15}	20u/1u

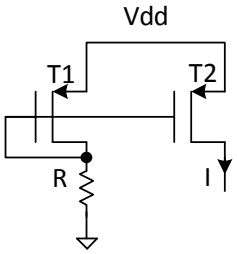

Fig. 3. The basic biasing circuit implementation

T1 and T2 transistor values are selected as 20µm/1µm. 100Ω resistance value is used for R. The layout of the voltage differencing trans-conductance amplifier is given in Fig. 4. The layout occupies 747.4µm area. The trans-conductance value for each floating current sources are same as given in Fig. 5.

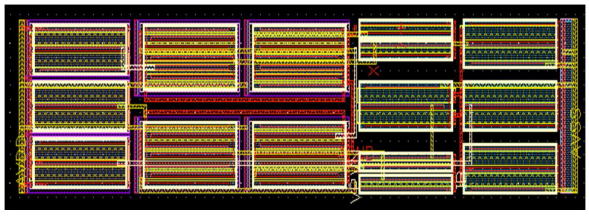

Fig. 4. The layout of the voltage differencing trans-conductance amplifier

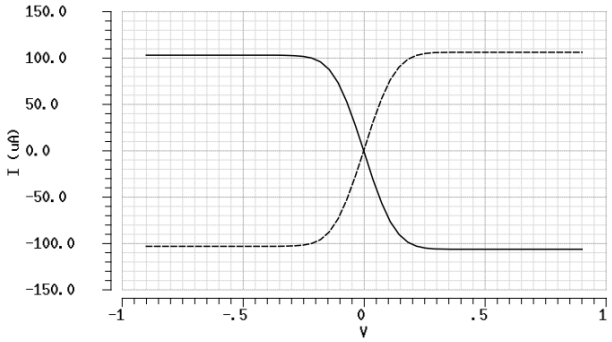

Fig. 5. The dc transfer characteristic of trans-conductance value

3. Frequency agile filter

Software defined radio, or SDR is based on the controllability of the frequency, bandwidths, modulation using computer tools [8]. Cognitive radio does not operate in a fixed band. The principle of the cognitive radio is improved by searching and using the suitable band. The adaptation of the any frequency, band-width, modulation, etc., is possible by the aid of the reconfigurable receiver.

Such architecture background designs require reconfigurable analog elements: LNA, local oscillators, mixers and filters [4]. Frequency agile filter's pass-band center frequency can be digitally adjustable.

Lakys and Fabre recently proposed that the second generation current controlled conveyor designed by Bi-CMOS (SiGE) technology is perfectly suitable for the realization of frequency agile filters. The controllability of the agile filter is implemented by the parasitic resistance at the X terminal of the second generation current conveyor. The different center frequency of the agile filter is obtained by changing the X terminal parasitic resistance related to the external biasing current. [3, 4].

Furthermore, the same technique is also considered to be used in passive radar receivers which are operate up to 1GHz frequencies.

In this work, frequency agile filter which has high operating frequencies is proposed by CMOS implementation. The CMOS implementation is a significant advantage of the designed VDTA voltage mode filter. In contrast to Bi-CMOS implementation, CMOS production is very cheaper. Thanks to floating current source's very basic CMOS implementation, the chip size occupies very less chip area.

Single block second order VDTA filter structure is given in Fig. 6. The designed frequency agile filter is built on the second order filter given in Fig. 6.

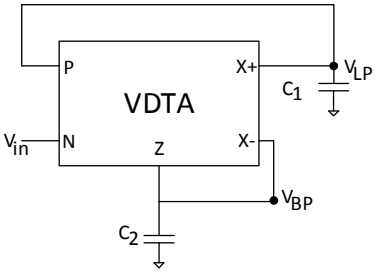

Fig. 6. VDTA second order filter structure

The filter structure has one band pass output section and one low pass output section at the capacitor C_2 and C_1 nodes, respectively. The transfer function of the low pass and band pass output are given in Equation 2 and 3, respectively. Equation 4 shows the pole angular frequency. Equation 5 gives the quality factor of the filter.

It can be easily seen that the center frequency can be changeable by C_1, C_2 capacitance. The quality factor of the filter will be fixed at the same time for equal change of C_1 and C_2 capacitances.

The MOS capacitor given in Fig. 7 are used to realize C_1 and C_2 capacitances. MOS capacitance is obtained by connecting the nMOS source, drain and bulk at the ground. At this time, all n-well behaves as capacitance. The capacitance increases by selecting big sizes W (width of nMOS transistor) and L (length of nMOS transistor) [5].

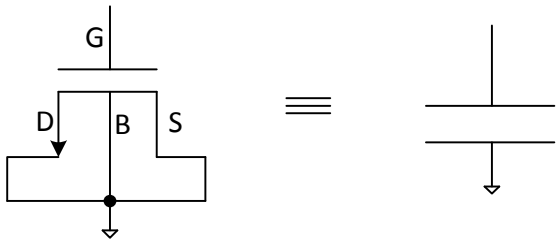

Fig. 7. MOS capacitor representation

The filter structure can be easily improved by using two cascaded second order filter to obtain fourth order filter.

Fig. 8 shows the frequency response of the filter for low pass and band pass output for 555MHz center frequency. There are a little gain loss which are acceptable for analog signal processing. Fig. 9 gives the transient response for the 555MHz input signal. Time domain response of the circuit is performed for 100 mV peak value at 555MHz sine wave.

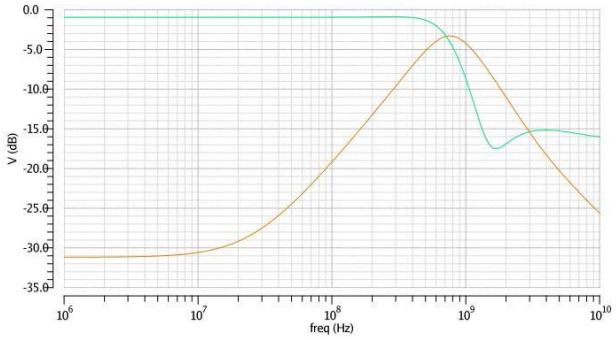

Fig. 8. Frequency response of the filter

$$\frac{V_{BP}}{V_{in}} = \frac{sC_1 g_{m1}}{s^2 C_1 C_2 + sC_1 g_{m1} + g_{m1} g_{m2}} \tag{2}$$

$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + sC_1 g_{m1} + g_{m1} g_{m2}} \tag{3}$$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{4}$$

$$Q = \sqrt{\frac{C_2 g_{m1}}{C_1 g_{m2}}} \tag{5}$$

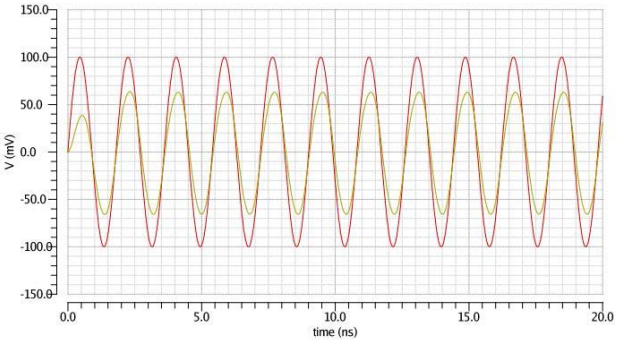

Fig. 9. Time domain response of the circuit for 100 mV peak value at 555MHz sine wave

The designed frequency agile filter is given in Fig. 10. The MOS-caps are shown as capacitor for easy demonstration in Fig. 10. The values of capacitors show the W(width) of the MOS-caps. The designed filter has good advantage because of single block. Also, the parasitic capacitance at the X- and X+ node is very suitable for good accordance for MOS capacitor. All MOS capacitor L (length) size are selected as 0.18µm.

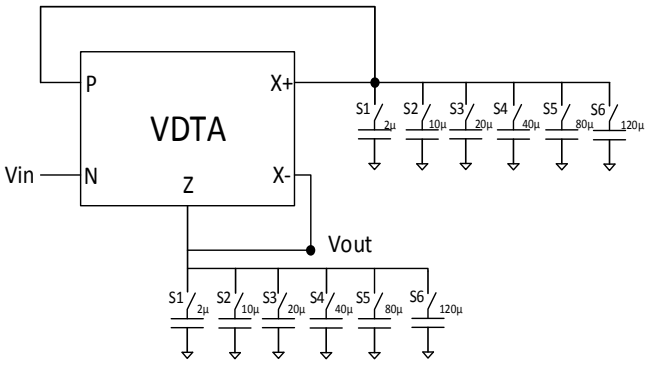

Fig. 10. The designed frequency agile filter

Fig. 11 shows the frequency agile filter output for different trans-conductance values. The quality factor of the designed agile filter is constant for all spectrum as shown in Fig. 11. The maximum operating frequency is obtained as 921MHz for 2µm W size.

The maximum output voltage harmonic distortion is measured as 1.2 % for 600mV input voltage amplitude at 555MHz center frequency.

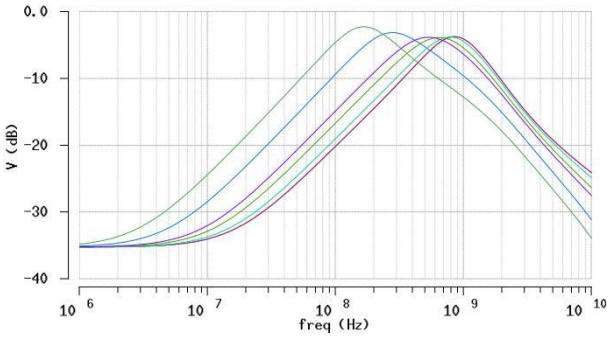

Fig. 11. Frequency agile filter output

4. Conclusions

A new frequency agile filter structure driven a single block voltage differencing trans-conductance amplifier is proposed in this paper. The main characteristics of the filter and VDTA are tested by the layout of the VDTA. The significant advantages of the agile filter is compared with some classical implementations. The floating current source used for CMOS implementation of VDTA and MOS capacitor technique provides perfect benefits in terms to operate at high frequencies. The layout and simulations are performed in CADENCE environment with 0.18µm AMS parameters.

5. References

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