An Ultra Low-Voltage Ultra Low-Power Memristor

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Abstract

Memristor can provide new approaches especially in nonlinear & chaotic circuit design. Since no commercially available memristor exist until yet, obtaining of a practical implementation which behaves as a memristor, is very important from the point of view real-world circuit design. In this work, an ultra low-voltage ultra low-power DTMOS-based design of memristor is presented. A new ultra low-voltage, ultra low-power operational amplifier and a new ultra low-voltage, ultra low-power multiplier are also proposed to use in the realization. Our design is composed of these two type active blocks using CMOS 0.18µm process technology with symmetric ±0.25V supply voltages. Characteristics and performance of our design is verified by PSPICE simulations. Total power consumption of the proposed memristor is found as just 4.3µW which is suitable for ultra low-power consumption. The simulation results show that our design provides the characteristics of memristor accurately and it could be a viable and convenient option especially in low-voltage low-power memristor based chaotic applications.

1. Introduction

In 1971, Leon Chua theorized memristor as the fourth circuit element beside the three well-known circuit elements such as resistor, capacitor and inductor [1]. Chua suggested that the memristor should have been accepted as a fundamental circuit element and it should have been added to the list of the basic elements in the circuit theory books. However, it has remained just as a theoretical element and has rarely appeared in the literature because of having no simple and practical realization.

In 2008, a group of researchers from HP laboratories led by Stanley Williams announced the fabrication of physical implementation of memristor [2]. Their prototype was based on a nanometer scale, TiO_2 thin film containing doped and undoped regions between two metal contacts. Physical model of memristor realized by HP researchers has attracted significant attention and afterwards many new studies have taken place in literature. Despite large-scale interest on memristor and emerging many studies, no commercially available memristor exists yet. A proper low-power low-voltage physical implementation representing the memristor is of great importance from the point of view real-world circuit design.

Various analog application of memristor, its SPICE macromodels and memristor emulators which have memristor-like behavior are presented in the literature [3-12]. It is possible to simulate memristor by using macromodels but they are not applicable on real applications. Emulators can represent the behavior of memristor in circuits; however they might have some limits in presenting actual circuit behavior. A fully CMOS based memristor design employing DDCC based circuit blocks is proposed by Yener and Kuntman [13].

This paper proposes an ultra low-voltage, ultra low-power memristor design especially for the memristor based chaotic applications. DTMOS (Dynamic Threshold MOS) transistors are used in the design of the sub-blocks of the memristor to effectively use the ultra-low supply voltage for ultra-low power consumption. In the design of sub blocks, DTMOS transistors are generated by connecting their gate and body terminals of PMOS transistors in standard n-well CMOS process where the bodies of PMOS transistors are externally available [14-15].

The paper is organized as follows: Section 2 summarizes the terminal relations and cubic modeling of memristor. Section 3 contains principles and characteristics of DTMOS transistor. Section 4 includes characteristics and details for operational amplifier (op-amp) and multiplier which are proposed in this paper. Section 5 is devoted to the demonstrations of SPICE simulations that are based on the proposed design. Finally in Section 6, the conclusion of this work is presented.

2. Properties, Terminal Relations and Modeling of Memristor

There are six possible combinations between charge, current, voltage and magnetic flux. All of these are well known except charge - magnetic flux. Last possible relationship has been defined by Chua as the fourth basic circuit element. Chua defined memristor with two type nonlinear constitute relation:

$$v = M(q)\,i \tag{1}$$

$$i = W(\varphi)\,v \tag{2}$$

Where M(q) and W(φ) are called memristance and memductance respectively and they are expressed by,

$$M(q) = d\varphi(q)/dq \tag{3}$$

$$W(\varphi) = dq(\varphi)/d\varphi \tag{4}$$

The memristor proposed in this work is a flux controlled memristor described by the relation in (5). The relation between the terminal voltage v(t) and the terminal current i(t) of the memristor is given by:

$$i(t) = \frac{dq}{dt} = \frac{dq}{d\varphi}\frac{d\varphi}{dt} = \frac{dq}{d\varphi}v(t) = W(\varphi(t))\,v(t) \tag{5}$$

Nonlinear resistor in Chua's circuit is defined by Zhong with cubic nonlinearity. It has been revealed that not all features of a real circuit are captured correctly by piecewise-linear definition [16]. A cubic nonlinearity is also chosen for the memristor implementation by Muthuswamy [17]. For the q-φ function of memristor with cubic nonlinearity:

$$q(\varphi) = \alpha\varphi + \beta\varphi^3 \tag{6}$$

Thus, the memductance function is given by:

$$W(\varphi) = \frac{dq}{d\varphi} = \alpha + 3\beta\varphi^2 \tag{7}$$

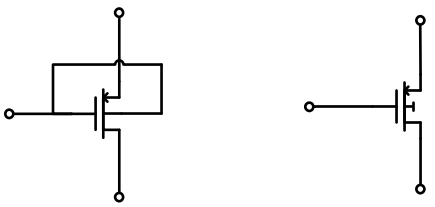
Considering (7) in (2) we get (8). The i-v function of memristor is defined as the relation given in (9). In this work, we use this relation in our design.

$$i(t) = W(\varphi)v(t) = \left(\alpha + 3\beta\varphi^2\right)v(t) \tag{8}$$

$$i(t) = \left[\alpha + 3\beta\left(\int v(t)\,dt\right)^2\right]v(t) \tag{9}$$

3. DTMOS Transistor

DTMOS transistor shows high threshold characteristic when it is off to minimize the leakage and it behaves as a low threshold device for high current drivability under low voltage supplies. DTMOS transistor is generated by connecting body of a regular MOS transistor to its gate terminal as shown in Fig. 1.



(a) (b)

Fig. 1. DTMOS transistor: a) view of gate-bulk connection, b) simplified circuit symbol

This configuration decreases the threshold voltage of the transistor because of the following relation (10) where γ is the body effect factor, ΦF is the Fermi potential.

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}\right) \tag{10}$$

Normally, source body junction of a MOS transistor is reverse biased which results in body effect and increases threshold voltage whereas in DTMOS technique this junction is forward biased to reduce threshold voltage. This reduction makes the device suitable for low voltage operation. As explained in [18], this reduction is arisen from the reduction of the body charge. The result is the increase in the inversion charge and the gate capacitance of a DTMOS transistor. Although gate capacitance increases in DTMOS transistor, performances of DTMOS circuits do not decrease because of the high current drive and higher carrier mobility. Higher carrier mobility in DTMOS transistor is induced by the reduction of the body charge which causes lower effective normal field in the channel [18].

4. DTMOS Based Sub-Blocks of Memristor

4.1. DTMOS Based Ultra Low-Voltage Ultra Low-Power Operational Amplifier

For the implementation of the memristor element, an ultra low-voltage low-power DTMOS operational amplifier is designed. DTMOS op-amp is composed of a DTMOS current mirror operational transconductance amplifier (OTA) and a simple inverter output stage. The topology is very compact and only 11 MOS transistors are used. DTMOS-based op-amp circuit is shown in Fig. 2 where M1-M5 and M10 are DTMOS transistors. M1 transistor supplies the biasing current of M4 and M5. M6-M7 and M8-M9 are the current mirror pairs. VB1 is the biasing voltage which can be changed to adjust the biasing current of the first OTA stage. In our application, we have chosen this biasing voltage as VB_1=-0.1V. Drain of the M9 transistor is the output of the initial DTMOS OTA stage which has high output impedance where the voltage signal is weak if low resistive loads are connected to the output. However this node sees the gates of M10 and M11 which are very high impedance inputs. Thus, voltage signal is transferred to the output where M10 and M11 increase load driving capability but the output stage is still incapable of driving low resistive loads and overall circuit behaves a kind of high output impedance circuit. This problem can be solved by applying additional negative feedback however this would require more circuitry which increases power consumption. In our application, using the available ultra low-voltage ultra low-power DTMOS OTA stage in [19] for the circuit in Fig. 2, it is sufficient in our memristor circuit when there is high resistive load connection at the output. CC is the Miller compensation capacitor. Choosing 8pF is sufficient for stability in our application.

In order to obtain ultra low-power consumption, all the transistors in the circuit are biased in the sub-threshold region where a MOS transistor current is given by the equation in (11).

$$I_D = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS} - V_{TH}}{nkT}\right)\left[1 - \exp\left(-q\frac{V_{DS}}{kT}\right)\right] \tag{11}$$

In this mode of operation, DTMOS transistors operate with an ideal sub-threshold swing of 60mV/dec. For simplicity, we have used an inverter based buffer output stage formed by M10 and M11. Transistor dimensions of the op-amp are given in Table 1.

Table 1. The proposed op-amp circuit transistor dimensions

Transistor	Width	Length
M1, M2, M3	5μm	2μm
M4, M5	300μm	2μm
M7, M8	50μm	5μm
M6, M9	100μm	5μm
M10, M11	400μm	2μm

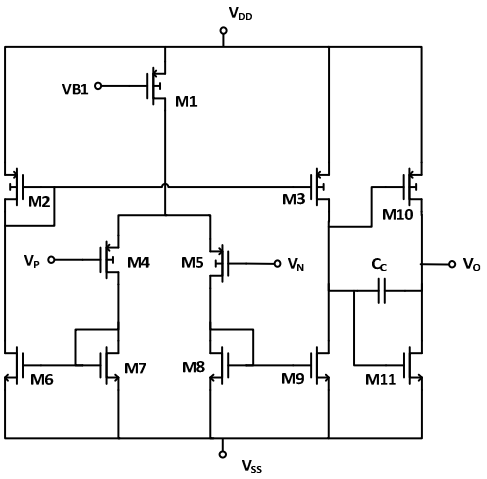


Fig. 2. DTMOS ultra low-voltage ultra low-power op-amp used in the memristor design

4.2. DTMOS Based Ultra Low-Voltage Ultra Low-Power Multiplier

Ultra low-voltage, ultra low-power DTMOS multiplier circuit is shown in Fig. 3. The circuit is supplied by ±0.25V symmetrical power supply. All transistors are operating in the sub-threshold region. The multiplier is based on four-quadrant sub-threshold multiplier in [20]. For ultra low-voltage operation, M5-M7 DTMOS transistors are added. To pick up the output current, M8-M9 and M10-M11 current mirror transistors are used and overall circuit is consist of only 11 transistors. VB_1 was chosen as -0.15V.

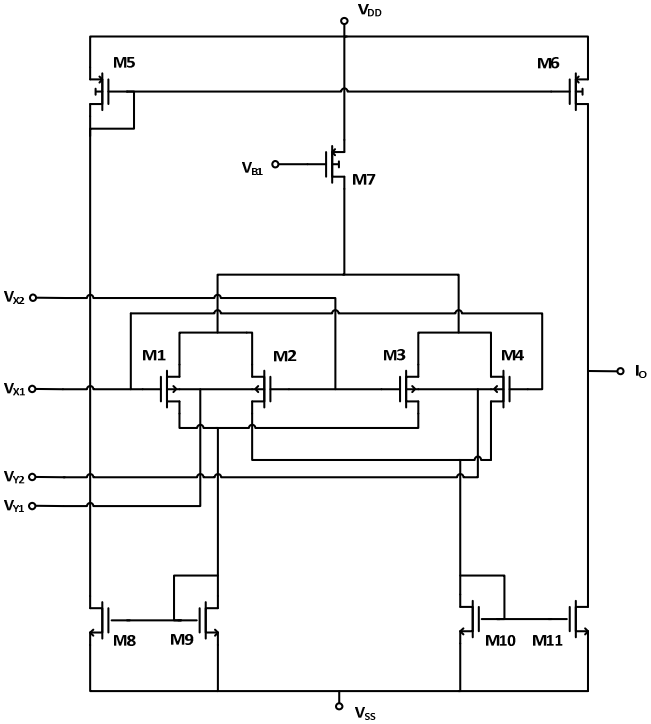


Fig. 3. DTMOS four-quadrant ultra low-voltage ultra low-power multiplier circuit used in the memristor design

Body terminals of M1-M4 are used for applying the input signal so the circuit can be also thought as a bulk-driven multiplier with additional DTMOS transistors. In fact, the structure is based on classical Gilbert multiplier and gives Gilbert-like multiplication coefficient. Output current can be approximated as

$$i_o = \frac{I_b \kappa(1-\kappa)}{4V_t^2} v_x v_y \qquad (12)$$

where κ is a process-dependent parameter, V_t is the thermal voltage and I_b is the biasing current flowing over M7 transistor. Multiplication constant is directly dependent biasing voltage and the W/L ratio of the M7. In our design we defined the dimension of M7 as W/L=8µm/2µm. It is possible to increase multiplication constant increasing the W/L of M7. Transistor dimensions of the circuit are given in Table 2.

Table 2. The proposed multiplier circuit transistor dimensions

Transistor	Width	Length
M1, M2, M3, M4	200µm	2µm
M5, M6	50µm	5µm
M7	8µm	2µm
M8, M9, M10, M11	50µm	5µm

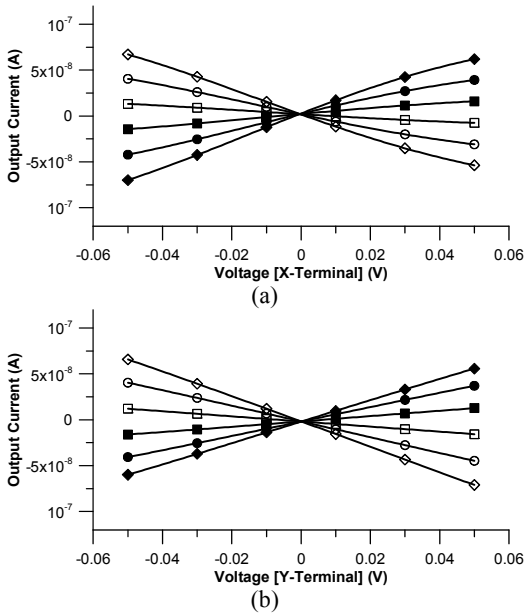


Fig. 4. DTMOS multiplier output current respect to input voltage. a) Io-V_X, (V_Y parameter -50mV...+50mV), b) Io-V_Y, (V_X parameter -50mV...+50mV)

5. Proposed Design and Simulation Results

5.1. Block Description of the Proposed Model

The block diagram of proposed memristor is given in Fig. 5. The memristor circuit employs only these DTMOS based operational amplifier and multiplier blocks which have ultra low-voltage operation characteristics. Negative and positive power supply voltages were set to just ±0.25V.

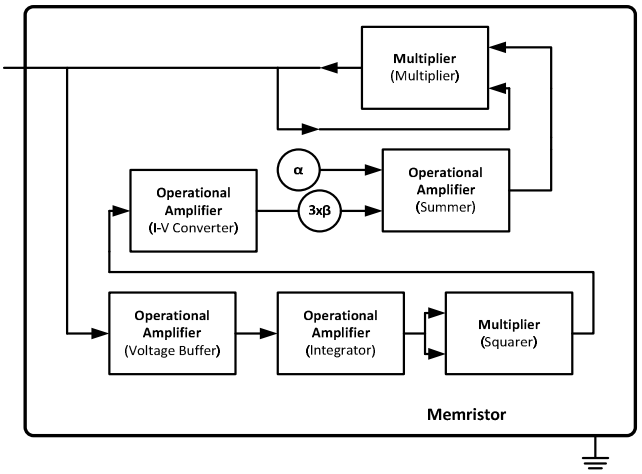


Fig. 5. Block schematic of ultra low-voltage, ultra low-power memristor design

Four op-amps and two multipliers are used in the design. As the first block, voltage buffer is used to avoid loading effect and insulate the current from the other stages. The second op-amp block works as the integrator. Here, in the integrators, a feedback resistor was used to prevent typical integrator saturation problem due to the offset. The output of the integrator is connected both of the inputs of multiplier and here it is the square of the voltage. Following two op-amp blocks make current-voltage conversion and summing operation which incorporate alpha and beta coefficients to the process. Finally, in the last multiplier block with buffered inputs, memristor current is generated after the output of op-amp multiplied by memristor voltage.

5.2. PSPICE Simulation Results

We have used ±0.25V symmetrical power supply. Limiting the maximum supply voltage level to 0.5V avoids parasitic diodes to turn on which may cause excess current flow through the source body, drain body junctions of DTMOS configuration. Additionally, excess currents in DTMOS transistor for the supply voltage levels over 0.5V causes problems for the usage of compact transistor models and may lead to unpredictable simulation results. For our memristor application, ±0.25V supply voltage was sufficient to satisfy our desired bandwidth above the kHz range and the performance of the memristor without causing any speed or bandwidth problems.

Fig. 6 shows the current and voltages against time and the current (I) – voltage (V) curve of the memristor at different frequencies. Memristor is driven by a 50mV sinusoidal voltage source with no offset voltage. Using ±0.25V supply voltages, with our design hysteresis behavior is observed at kilohertz-levels which is suitable to chaotic circuits. Total power consumption of the proposed memristor circuit is given by SPICE as just 4.3µW which is suitable for ultra low-power consumption.

The hysteresis loop of the memristor is not a curve which indicates the operating characteristics entirely. However it is an essential and commonly referred characteristic to illustrate memristor characteristics. The simulation results are compared with the theoretical results, thus the performance and the accuracy of the model have been proved.

6. Conclusion

In this paper, we propose an ultra low-voltage and ultra low-power design of memristor. Also a new ultra low-voltage and ultra low-power op-amp and multiplier are presented and used in the design. The proposed memristor is defined with cubic polynomial function where the charge is a cubic form of the flux. The accuracy of the proposed blocks and characteristics of the memristor are observed by PSPICE simulations. Experimental results are presented comparing with theoretical results and performance of the design has been demonstrated. Total power consumption of the proposed memristor with ±0.25V supply voltages is found as just 4.3µW which are suitable for ultra-low power ultra low-voltage attributes.

The proposed circuit is the first approach on a working low-voltage, low-power design of memristor. Since no manufactured memristor is available yet on the markets, the circuit proposed exhibits high importance for correct modeling and low-power, low-voltage applications of memristor. We believe that our memristor design would benefit the implementation of low power memristor-based circuits and it can be considered as a further contribution to low-voltage, low-power chaotic and analog signal processing applications.

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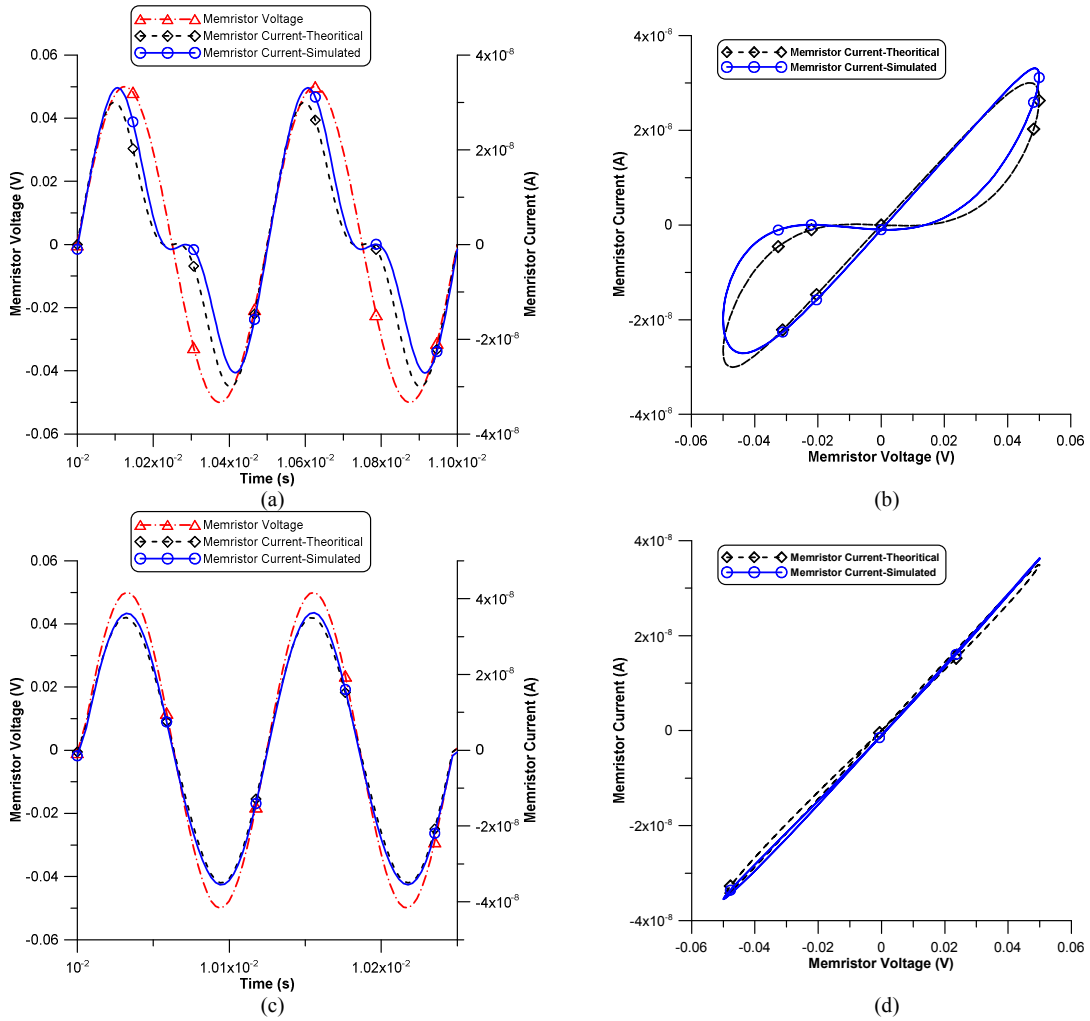

Fig. 6. Time-domain current and voltage waveforms and corresponding pinched hysteresis loops recorded from the circuit vs. theoretical results at various frequencies. a), b) at 2kHz, c), d) at 8kHz.

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