A New Neuron Model Suitable for Low Power VLSI Implementation

Ozgur Erdener[1], Serdar Ozoguz[2]

1 Istanbul Technical University, Graduate School of Science,
Engineering and Technology, 34469, Maslak, Turkey
erdener@itu.edu.tr
[2]Istanbul Technical University, Faculty of Electrical-Electronics Engineering,
34469, Maslak, Turkey
ozoguz@itu.edu.tr

Abstract

This paper presents a new dynamical neuron model which is appropriate for electronic circuit implementation and its low power, compact VLSI implementation. The neuron circuit consists of one first-order log domain filters, hyperbolic type nonlinear function generator and resetting circuitry. Owing to the log domain design and current-mode operation in a 0.35 µm CMOS process, the circuit occupies low chip area and has very low power consumption during real time scale operation. These features make the circuit suitable for hybrid interface applications and large scale VLSI neuromorphic networks.

1. Introduction

We constantly receive and process sensory input from our environment and recognize food or danger and take the appropriate actions with apparent ease. The reason of this performance lies in our neural structure or brain [1]. Complex tasks such as vision processing, decision-making, motor control and so on can be performed by brain in a very fast and energy efficient way. The brain performs these tasks utilizing massive parallelism, distributed storage, asynchronous processing, self-organization and synchronization. [2].

Today we still do not have sufficient knowledge about how the whole brain works but there is detailed knowledge about the structure and functionality of small portions of the brain.

In traditional artificial neural networks, the neuron behavior is described only in terms of firing rate, but most of the real neurons, commonly known as spiking neurons, transmit information by pulses (i.e. action potentials or spikes). Spiking neuron models vary from the computationally simple Integrate and Fire (I&F) model to biologically meaningful Hodgkin-Huxley (HH) model. According to accuracy requirements and electronically eases of implementation the appropriate neuron model is selected.

Today's understandings and methods of modeling the neuronal behavior have been significantly influenced by the work of Hodgkin and Huxley [3]. The proposed neuron model's parameters are biophysically meaningful and measurable but extremely expensive to implement. Because of the complexity of the Hodgkin-Huxley model (HH), reduced models have been proposed. In 1961, FitzHugh has investigated the phase portraits of HH by using bifurcation parameters and proposed a simpler model called FitzHugh-Nagumo Model [5]. In 1984 Hindmarsh and Rose reinvestigate the FitzHugh-Nagumo model and proposed 3th degree Hindmarsh-Rose equations [4] by fixing the insufficiencies of this model. There are also models that combine continuous spike-generation and a discontinuous 'after-spike' reset of state variables [13]. These are called hybrid neuron models [8], [9]. After these seminal works, many neuron models were proposed that explains the spiking behavior of a single neuron cell [4-10].

While the goal of Hodgkin-Huxley-type conductance-based models are matching the neuronal electrophysiology with biophysically meaningful and measurable parameters, hybrid models aim to match the neuronal dynamics with mathematically meaningful state equations.

In this paper, we focused on the dynamics of a single neuron cell (even including more realistic compartmental model) and offered a new hybrid type neuron model which completely appropriate for electronic circuit implementation.

2. Proposed Model

A common feature of various two-dimensional neuron models is having a fast membrane voltage variable and a slower adaptation current variable. Typically, the fast variable has an N-shaped nullcline and the slower variable has a sigmoid or linear shaped nullcline [11]. Morris-Lecar [15] and FitzHugh-Nagumo [5] is the two most important examples to these models. Also the combination of an after-spike reset mechanism with these features is used to obtain a rich dynamic behavior and spiking repertoire.

By using the above facts we offered a new neuron model. The main motivation was to design a model which is completely appropriate for low power and compact VLSI circuit implementation. To this end, we used an odd symmetrical nonlinear function which is more suitable for circuit implementation. Therefore, new model is constructed with tangent hyperbolic functions since it is odd symmetric and easily implementable as VLSI circuit.

The proposed model is given below:

$$\begin{aligned} \tau_x \frac{dx}{dt} &= X_1 \tanh\left[\left(x + X_o\right)X_{sy}\right] - X_2 \tanh\left[\left(x + X_o\right)X_{sx}\right] \\ &\quad - y + Y_{in} \\ \tau_y \frac{dy}{dt} &= Y_1 \tanh\left[\left(x + X_o\right)X_{sy}\right] - y + Y_2 \\ x > X_{max} &\Rightarrow x \leftarrow X_r \end{aligned} \tag{1}$$

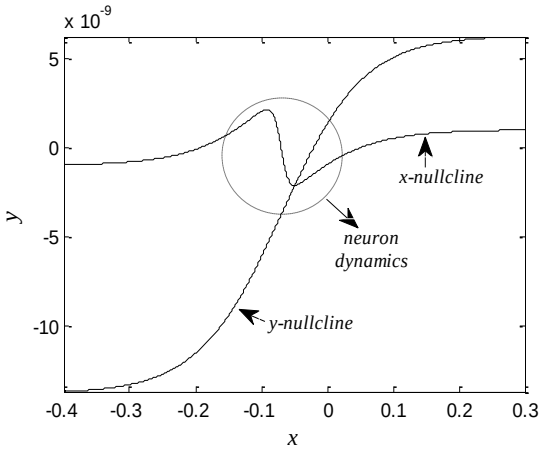

Fig. 1. Nullcline derivation of the new neuron model. Fast (x) and slow (y) variable nullclines are obtained by scaling the tangent hyperbolic functions. Neuron dynamics takes place in the N-shaped are marked with dotted circle.

where $x(t)$ and $y(t)$ are the state variables that mimic the membrane potential and the recovery of membrane potential, respectively. The latter one corresponds to activation of K^+ ionic currents in $IN_{a,p}$+IK model.

As shown in Fig. 1, for the N-Shaped nullcline we scaled two tangent hyperbolic functions (i.e. $p_1\tanh(p_2x) - p_3\tanh(p_4x)$]) and for sigmoid(linear)-shaped nullcline, we scaled one tangent hyperbolic function (i.e. $p_5\tanh(p_2x)$).

In Table 1, we give some illustrative parameter set values for different dynamical behaviors where $Y_1=10^{-8}$, $Y_2=3.27.10^{-9}$, $X_2=3.10^{-9}$ in all the cases.

Table 1. Parameter values of various spiking patterns obtained with offered neuron model.

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Dynamics	τ_x	X_1*	X_{sx}	X_{sy}	X_o	τ_y	X_r
Limit Cycle	1.5e-11	3.5	80	8	0.07	0.025	-
Tonic Spiking	1.5e-11	4	80	8	0.07	0.060	-0.04
Tonic Bursting	1.5e-11	4	80	8	0.07	0.060	-0.03
Class-I Excita.	1.5e-11	4	80	8	0.07	10	-0.05
Class-II Excita	1.5e-11	4	80	8	0.07	0.040	-0.04
Integrator	1.5e-11	4	80	8	0.07	0.035	-0.05
Resonator	1.5e-11	5	80	8	0.07	0.003	-0.05
Spiking	3e-12	4	16.5	1.5	-0.6	0.023	0.70
Bursting	3e-12	4	16.5	1.5	-0.6	0.023	0.82

* to be multiplied by 10^{-9}.

3. Proposed Model

As we explained in the previous sections, the main advantage of our neuron model is suitability for low power and compact electronic implementation. In our design, the variable $x(t)$ is realized as a voltage quantity while the variable $y(t)$ is represented as a current. All transistors, except for those used in the current reference circuit, operate in subthreshold region to satisfy the low power condition.

The circuit is designed using TSMC 0.18um technology, which is an n-well process, where the body effect is effective in inner layer transistors. Because the circuit operates at picoamperes range, the minimum channel width to length ratio (i.e. W/L) is chosen as 2um/2um for minimizing the effect of the absolute parameter deviation due to VLSI manufacturing process. The supply voltage is chosen as 1.5V for being compatible with the equipments operating with battery.

In the sequel, subcircuits of the overall neuron circuit are briefly explained.

3.1 Tangent Hyperbolic Block (THB)

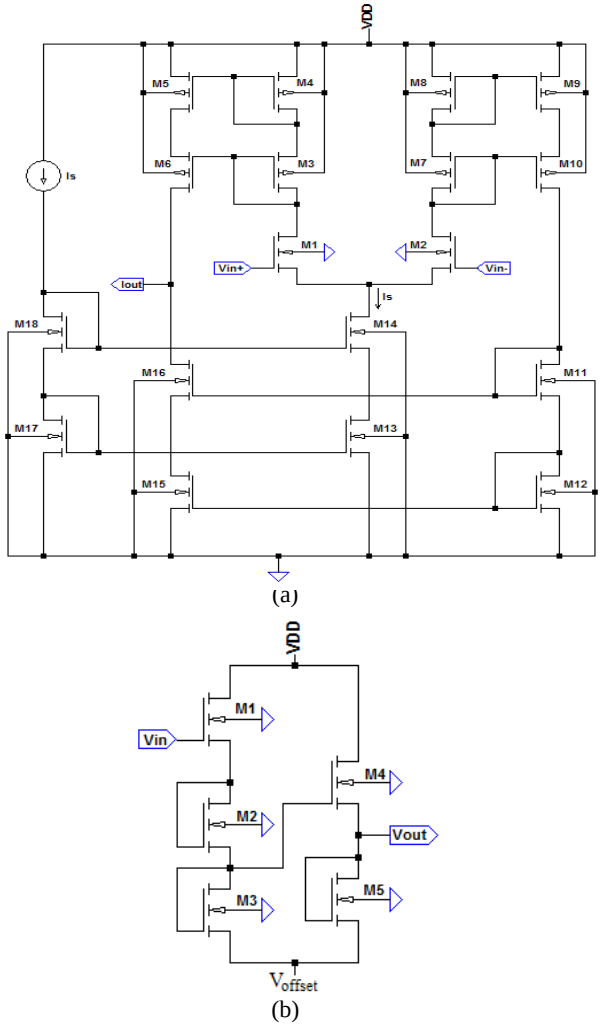

Fig. 2. a) Source coupled pair with cascode output stage used as the Tangent Hyperbolic Function generator. b) 2-layered ladder type diode connected linear voltage divider with offset (V_{offset}=0.2 V).

THB is realized using a source coupled pair with cascode output stage as shown in Fig. 2a. By using subthreshold drain current equation in saturation, differential output current can be expressed as:

$$I_{out} = I_S \tanh\left(\frac{\alpha}{2}\left(V_{in+} - V_{in}\right)\right) \quad (2)$$

A voltage tunable current reference circuit is designed in order to eliminate the effect of process parameter variations on the circuit function. Tuning voltage varies for different current values, since there is no linear dependency between process parameter variations. That means, different tail current values in THB blocks- which is the case for our design- may need different tuning voltages. To prevent this situation, we designed a core THB with minimum tail current and then multiplied the output by a constant value for obtaining the real output of

different THB's. Tail currents are generated from a matched 100pA current sources.

As it can be seen from equation (2), intrinsic architecture of the circuit dictates the value of X_{sx} as α/2 and the ratio of two parameters, X_{sy} and X_{sx} should be of the order of 10. Since α is an intrinsic parameter, it is not possible to divide it but we can divide the input voltage to create the same effect. For this purpose, we designed a two layered ladder type diode connected linear voltage divider with offset as shown in Fig. 2b. If we ignore the body effect and channel length modulation, input-output relation of the circuit is given as:

$$v_{out}(t) = \frac{v_{in}(t) + 5V_{offset} + \frac{2}{\alpha} ln\left[R_1^{\,2} / R_2 R_3\right]}{6} \tag{3}$$

Comparing this with the conventional MOS voltage divider, two layered configuration has the advantage of having less number of transistors for the same divider value and of having reduced body effect. Offset voltage is needed to hold the output voltage above a certain value which should be high enough for proper operation of THB even at lower input voltages. Because the same offset voltage is applied to the both inputs of THB, its effect is eliminated in overall function as it can be seen from (2). For perfectly matched transistors, voltage divider provides a division factor of 6.

3.2 Current-Mode Log Domain Filter

If we get $y(t)$ as output and Y_1 tanh[$(x\text{-}X_o)X_{sy}$] as the input at second state equation in (1), this expression corresponds to a typical first order low pass filter. This block can be represented as a log domain filter which is a useful block employed in neuromorphic circuits. For this purpose subthreshold operating translinear MOS circuit given in [27] has been used. The circuit schematic is shown in Figure 9. Using translinear principle, we can easily show that the state equation of the log domain filter is given by:

$$C\frac{dI_{out}}{dt} = I_{in}(\alpha I_b)\left(\frac{R_2 R_4}{R_1 R_3}\right) - I_{out}(\alpha I_d) \tag{4}$$

Here α is intrinsic parameter, thus can not be manipulated in the circuit design phase. Alternatively, we can manipulate I_b and I_b+I_d current sources, C capacitor value and the aspect ratios given as R_1, R_2, R_3, and R_4. The circuit is designed by setting these parameters to suitable values and the simulation results thus obtained shown in Fig. 4 verify the circuit's proper operation.

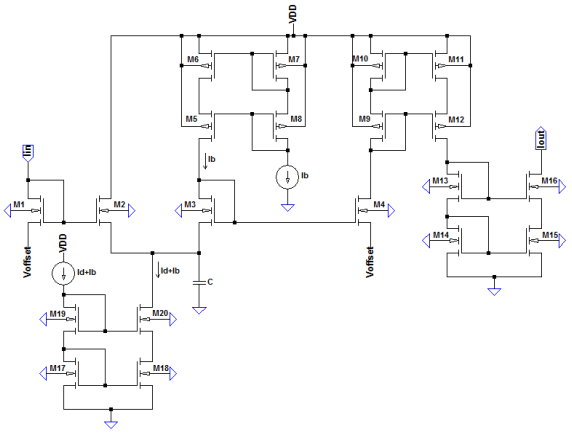

Fig. 3. Current-Mode Log Domain Filter.

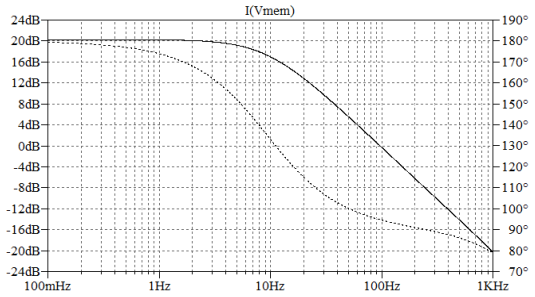

Fig. 4. Gain and phase response of log-domain filter with typical process parameters set (TT).

3.3 Current Reference Circuit

Process parameter variation and temperature dependency are the two most critical problems effective on the circuit operation. Especially, for the circuits based on subthreshold operation, temperature dependency is a very common problem.

Effect of process parameter variation is minimized by making the current reference circuit voltage tunable. The main blocks of our design, i.e. THB and Log Domain Filter have intrinsic dependency to the temperature because of $\alpha \propto \frac{1}{T}$ as can be seen in Eqns. (3) and (4). For current mirrors, there is no temperature dependency theoretically, if we ignore the CLM and body effects. Those issues mean that for temperature optimization we could only manipulate the bias currents. So the dependence of constant currents I_S (i.e. tail current of the core THB, see Fig. 2), I_b, and I_b+I_d (see Fig. 3) to temperature should be as low as possible in a reasonable temperature range. This makes the current reference circuit the most critical part of our design. We used the circuit in Fig. 5 which is a modified version of the current reference circuit presented in [28].

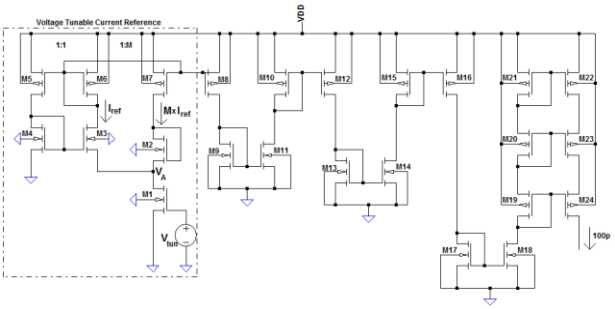

Fig. 5. Voltage tunable current reference and divisor current mirror circuits.

Routine analysis of the circuit leads to the reference current equation as follows:

$$I_{ref} = \mu_n C_{ox}\frac{R_1}{M+1}(V_{tun}-V_{th})V_A = \mu_n C_{ox}\frac{R_1}{\left(\frac{R_2}{R_S}+1\right)}(V_{tun}-V_{th})nU_T \ln\left(\frac{R_3}{R_4}\right) \tag{5}$$

where μ_n is the carrier mobility, C_{ox} is the gate-oxide capacitance and V_{th} is the threshold voltage. The first order definition of temperature dependent parameters in equation (10) are:

$$U_T = \frac{k}{q}T \quad ; \quad V_{th} = V_{th0} - \kappa T \quad ; \quad \mu_n = \mu_{n0}\left(\frac{T}{T_0}\right)^{-m} \tag{6}$$

where, V_{th0} is the *0* Kelvin (K) threshold voltage, κ is the temperature coefficient (TC) of V_{th0}, k is the Boltzmann

constant, q is the electron charge, μ_{n0} is the mobility at T_0, K and m is the mobility temperature exponent with an approximate value of *1.5*.

By substituting these expressions into the Eqn. (5), temperature coefficient of the reference current, I_{ref} as follows:

$$TC_{I_{ref}} = \frac{1}{I_{ref}} \frac{dI_{ref}}{dT} = \frac{2-m}{T} \quad (7)$$

Temperature dependency curves of three main biasing currents are shown in Figure 12. From these results, we can say that the temperature dependencies of currents are within a reasonable range.

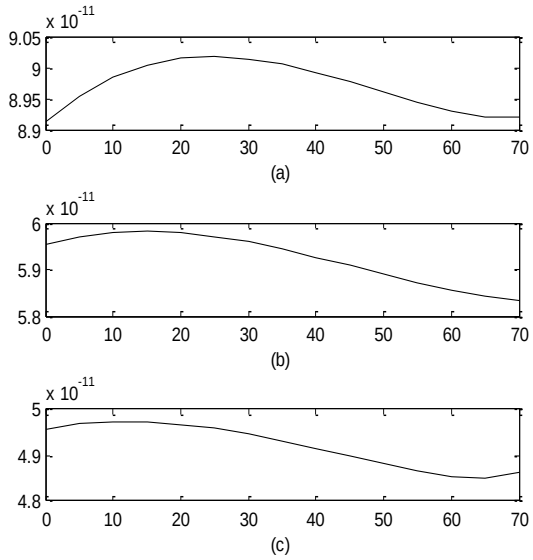

Fig. 6. Temperature dependence of critical currents in neuron circuit for simulation with typical process parameters set (TT). Horizontal axis is temperature in degree (^{0}C), vertical axis is current in Ampere (A) (a) Tail current of the core THB (b) I_b+I_d in Fig. 3 (c) I_b in Fig. 3.

3.4 Compare & Reset Circuit

For resetting the membrane voltage value we should discarge the membrane capacitance until its voltage decreases to V_R . For this purpose we should design a comparator circuit which drives a discharge switch with high current capacity. Designed circuit is shown in Fig. 7. This circuit implements the last expression in Eqn. (1).

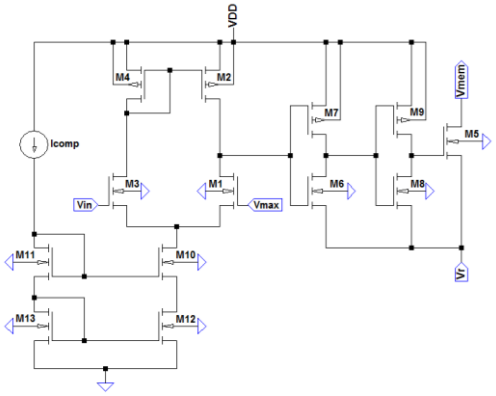

Fig. 7. Compare & Reset Circuit Schematic.

3. Simulation Results

The overall neuron circuits are realised using the main blocks already explained in the previous sections. Constant current source I_c is determined as *1.2 nA* in the overall design. Simulation results for typical process parameters (TT) is shown in Fig. 8. We obtained tonic spiking for V_R=*0.7V* and I_{in} =*105 pA* and tonic bursting for V_R=*0.82V* and I_{in} = *130 pA*.

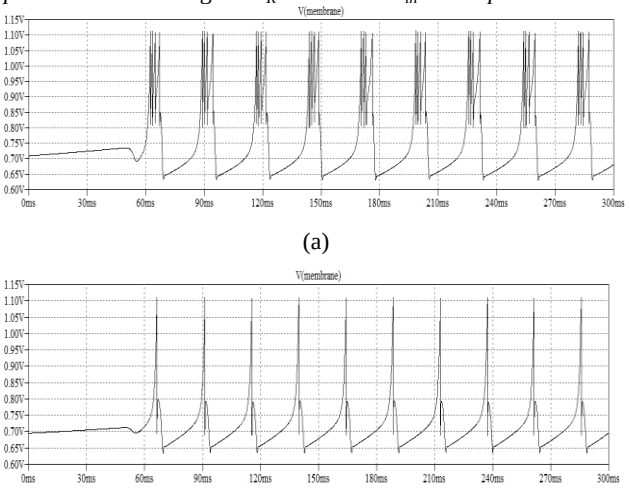

Fig. 8. Simulation results of the designed neuron circuit (a) Tonic Bursting (V_R= *0.82V* and I_{in} = *130pA*) (b) Tonic Spiking (V_R= *0.70V* and I_{in} = *105pA*)

Average power consumption of designed neuron circuit is found *241 nW* which meets the low power requirement. Comparison between our design and some other similar designs are given in Table 2.

Table 2: Comparison of the main parameters between our design with similar topologies.

	Power,nW	**Biological Timescale Factor**	**Spike Shape Conformity**	**Model**
[25]	7	x10	not fair	Izhikevich
[26]	100	x10^4	good	AdEx I&F
[29]	20	x1 (real)	good	Izhikevich
[30]	40	x10^4	good	Modified Izhikevich
[31]	70	x1(real)	not fair	Mihalas-Niebur
This paper	241	x1 (real)	very good	Our Model

4. Conclusion

In this work, a low power, real time implementation of a new neuron model is presented. Design procedures are explained and typical firing patterns of a cortical neuron are provided. Owing to the low power and real time operation capability, the neuron circuit suitable for building human interface electronics systems. Since the neuron relies on a mathematical model, it is possible to design large scale VLSI networks as a hardware simulation tool for computational neuroscience.

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