A New Fast and Accurate Current-Mode Folding Amplifier

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Abstract

In this paper we present a current mode saw-tooth folding amplifier with a minimal number of current mirrors in the signal path from input to output. This minimizes the delays imposed by current mirrors on the speed of the amplifier. The amplifier has a full scale delay of 5.9ns which is more than four times faster than presented in previous literature. The operation is verified in simulation using LFoundry 150nm process in Cadence Tools

1. Introduction

Analog to digital converters (ADC) are one of the most important sub-circuits of any digital systems which are intended to interface with the analog world. Because of their ubiquitous presence, ADCs with high speed, compact, low voltage and low power are highly desirable. There are different architectures of ADCs available in the literature among which full flash ADC is the fastest and simplest one. However, this kind of ADCs requires $2^N - 1$ comparators and 2^N resistors, where N is the number of bits, which causes such topology to be impractical for higher number of bits. One of the solutions is folding ADC which reduces the number of comparators and hence power and size of the ADC with a minimum compromise in the conversion speed. Folding ADCs require folding amplifier, and for the accuracy of conversion, saw-tooth folding characteristics is highly desirable. Moreover, current mode implementation can offer low voltage and faster response [1]. Thus, current mode folding amplifiers with saw-tooth transfer characteristics and faster response are of interest.

Conventional voltage mode folding amplifiers are built around differential amplifiers. Different folding ADCs reported in [2, 3, 4, 5] utilized voltage mode folding amplifiers which had either sinusoidal or triangular folding characteristics. Folding ADC with such folding characteristics causes error in digitization [6] and needs extra error correction/compensation circuitry. Moreover, these works will not be suitable for low voltage application due to the non-linearity of the differential amplifiers used for folding amplifier realization. However, folding amplifiers reported in [7, 8] offered saw-tooth transfer characteristics in voltage mode but were subjected to exact voltage generation which will require extra power management circuitry.

On the other hand, very few current mode folding amplifiers are found in literature. Current mirror based folding amplifiers reported in [9, 10] have triangular transfer characteristic which would cause conversion error in ADC application. Another current mode folding amplifier reported in [11] used current steering technique which also reported a sinusoidal transfer characteristics. The only current-mode folding amplifier with saw-tooth transfer characteristics was realized by two circuit blocks[12]: one for producing linear portion and another one for the sharp transition of the saw-tooth. However, the sharp transition was realized using large transistors (for large mirror ratio) which was causing slower response of the overall folding amplifier. A regeneration of the folding amplifier in [12] shows response time of about 235ns with $0.35\mu m$ technology which will be a major drawback to high speed folding ADC realization.

In [13] the authors presented a new design for a current mode folding amplifier which reduced the response time to 25ns. However it is observed that the main bottleneck in current mode folding amplifier design, is current mirrors in terms of speed and accuracy. Current mirrors especially when switching OFF or ON require discharge of the large pair of gate-source capacitances ($2C_{GS}$). As such it is desirable to reduce the number of mirrors in the signal path between input and output.

This work presents a folding amplifier which has a minimal number of mirrors in the signal path from input to output. The circuit was designed in $150nm$ LFoundry technology. The full scale delay from input to output delay is 5.9ns which is about four times better than the highest reported in the literature [13]. The rest of this paper is in two sections: Section II presents the folding amplifier block diagram and the circuits implementing the blocks. Section III discusses the simulation results of this amplifier. The paper is concluded in Section IV.

2. Folding Amplifier Design

A folding amplifier based ADC system is shown in Fig. 1. A folding amplifier is characterized by the number of folds, N, and the fold size I_F. Conceptually, the folding amplifier maps the input into the output in a modulo division fashion [14, 11]. If the signal is larger than the fold size, then I_F is repeatedly subtracted from it till it is smaller than the fold size. This leads to a saw-tooth characteristic as shown in Fig. 2. To realize such characteristics two elements are required: mirroring the input to output and subtracting the value once the input is beyond certain points. These points are of course: $I_F, 2I_F, 3I_F, \ldots, (N-1)I_F$ for an N fold amplifier.

The proposed folding amplifier is shown in Fig. 3. It is a straight forward implementation of the modulo division concept described in the previous paragraph. The amplifier has two inputs: the input current signal I_{IN} and the reference current I_{REF}. The fold size in this case is $I_F = I_{REF}/N$. The two

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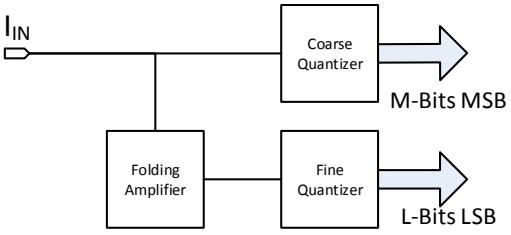

Figure 1. Folding Amplifier based

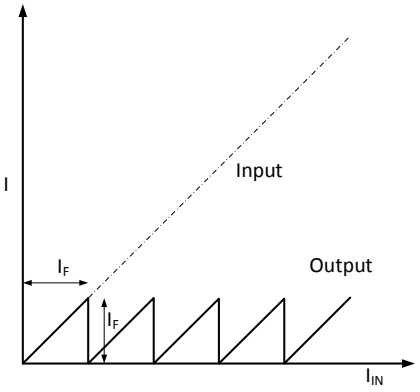

Figure 2. Input Output Characteristics of Ideal Fivefold Folding Amplifier: Input (dotted), Output (Solid) I_F is fold size

currents are fed to two mirroring and scaling circuits, the current copier and the reference scaler. The current copier produces N outputs: $N-1$ copies are shown as I_{CP} in Fig. 3 and one copy as I_X which goes directly to the output. The current scaler produces $2(N-1)$ outputs: $(N-1)$ that are scaled as $I_{REF}/N, 2I_{REF}/N, \ldots, (N-1)I_{REF}/N$, which are shown as I_{SC} on the diagram. The other $(N-1)$ outputs are all I_{REF}/N and are shown as I_Y on the diagram. I_{SC} and I_{CP} are subtracted from each other at the entrance of the comparators which compare whether the resulting currents are greater or less than zero, effectively giving $B[i] =$ logic 1, for $I_{CP}[i] < I_{SC}[i]$ for $i = 1, 2, \ldots, N-1$. The binary signal $B[i]$ is used to switch on/off the i^{th} transmission gate (shown as TGate) which subtracts a current $I_F = I_{REF}/N$ from the output, hence realizing folding. Notice that only one current mirror separates the input signal from the output.

The circuits used to realize these blocks are shown in Fig. 4. Instead of using large channel length transistors in mirrors as in [13] a folded cascode mirror is used for all mirroring [15]. This allows the use of smaller channel length transistors (300nm for all mirroring transistors) while not sacrificing the accuracy (all mirrors give less than 2% error in simulations for currents from $1 - 32\mu A$). For the current scaler the I_Y output terminals are not shown as they are similar to those used in the current copier. The cascode transistors are biased by a transistor which is half the width of the main transistor and biased by $I_{CAS} = 35\mu A$.

A well-known option for current comparison is the Traff comparator[16]. However the Traff comparator produces large delays for low currents (less than 0.5u, this was found through

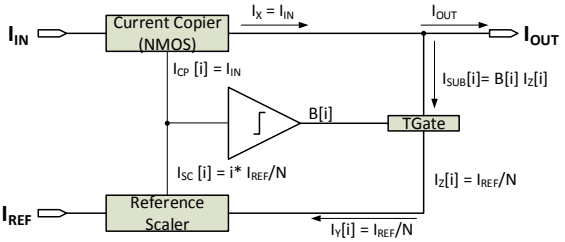

Figure 3. Block Diagram of Proposed Minimal Current Mirrors Count Folding Amplifier. Note that $i = 1, 2, ..., (N-1)$

simulations). For the current comparator we used the comparator reported in [17] which provides low input impedance, a small threshold current (50pA as reported in [17]) which is needed for accurate comparison. The inverters were sized so as to set the feedback connected inverter around mid-supply point. This was $1\mu m/150nm$ for the NMOS and $3\mu m/150nm$ for the PMOS. Transistor sizes are shown in Table. 1

Table 1. Transistor Sizes

Transistor	Size
Current Copier	
Cascode Bias	500nm/320nm
MCA, MNA	1000nm/320nm
Current Scaler	
Cascode Bias	500nm/300nm
MCA, MNA	8000nm/300nm
MC1, MN1	1000nm/300nm
MC2, MN2	2000nm/300nm
...	
Transmission Gate	
MPG	500nm/150nm
MNG	320nm/150nm
Current Comparator	
Inverter NMOS	1000nm/150nm
Inverter PMOS	3000nm/150nm
C_C	100fF
R_C	1.6KΩ

3. Simulation Results

The proposed folding amplifier was simulated in LFoundry $150nm$ process with a supply of $V_{DD} = 1.8V$. To compare with [13], a folding amplifier with $N = 4$ was designed, with a fold size of $4\mu A$ and with a load resistance of $10K\Omega$ connected to mid-supply ($V_{DD}/2 = 0.9V$). The input output relationship is shown in Fig. 5. This was obtained by performing a DC sweep of the input current from $0 - 20\mu A$ at a step of $50nA$. The error between the ideal and the simulated characteristics is shown in Fig. 6. The spikes are the misalignment of transition points from the ideal values of $4, 8, \ldots, 20\mu A$. Ignoring the misalignment of the switching points from the ideal values, the maximum error is less than $0.07\mu A$ at an input current of $20\mu A$.

To test the response time of the amplifier, a rising full-scale pulse signal (from $0\mu A$ to $20\mu A$) and falling full-scale pulse signal from ($20\mu A$ to $0\mu A$) are applied. These are shown in Fig. 7(a) and Fig. 8(a) respectively. The comparator outputs

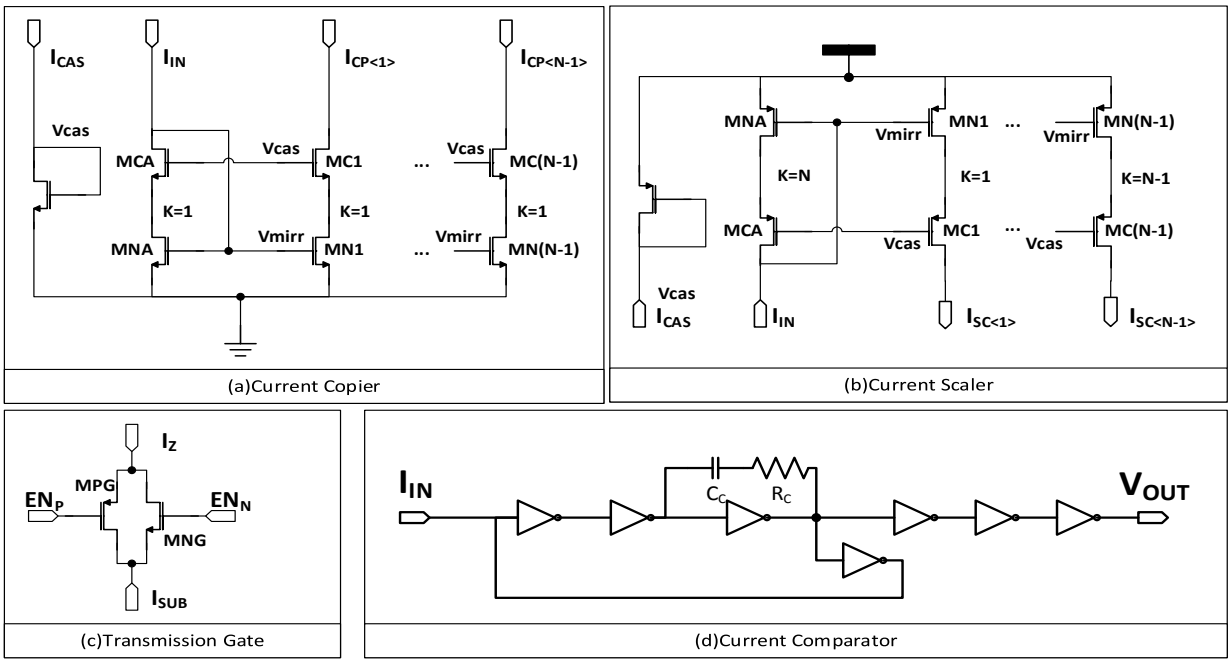

Figure 4. Circuit Level Implementation of Folding Amplifier Blocks: (a) Current copier (b) Reference Scaler (c) Transmission Gate (d) Current Comparator

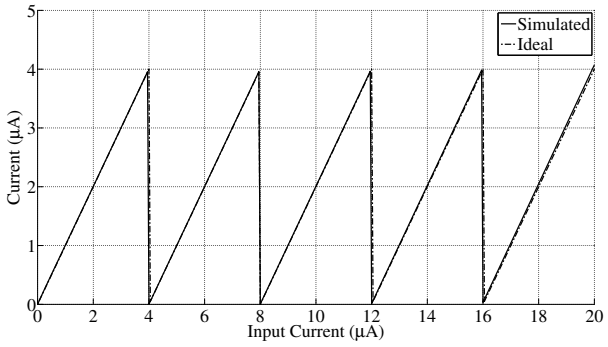

Figure 5. Input/Output Characteristics of the Folding amplifier: Simulated (Solid) Ideal (Dash-dot)

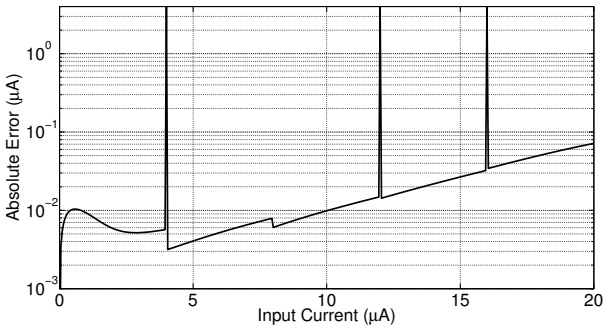

Figure 6. Absolute Difference (Error) between Simulated Characteristics and ideal characteristics.

are shown in Fig. 7(b) and Fig. 8(b) respectively. Notice that the falling pulse settled much faster than the rising one. Also we can notice very clearly in Fig. 7(a), the sudden jumps due to mirrors being switched on, which correspond to the switching instances in Fig. 7(b).

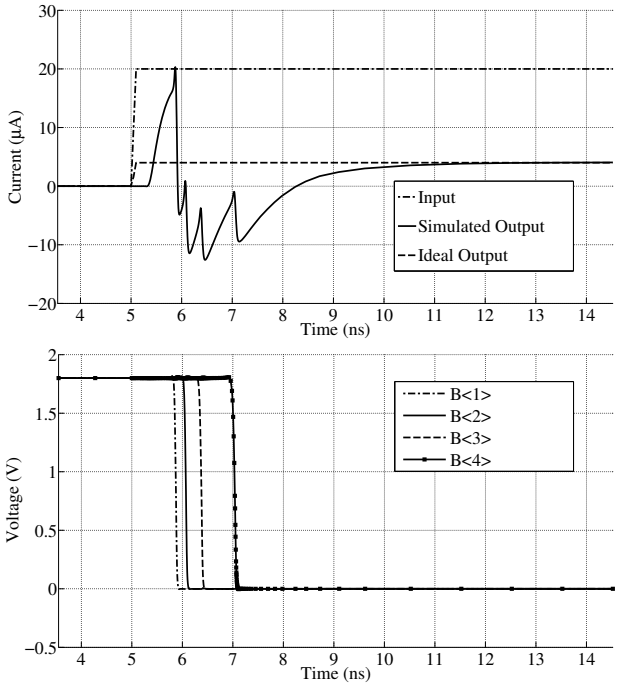

Figure 7. Transient Response for a Full Scale Rising Pulse

The 2% settling time was found to be $5.9ns$ for the rising pulse and $2.3ns$ for the falling pulse. Using the full scale delay there is a fourfold improvement of speed over [13]. All the comparators settled in atmost 2ns while the main current mirror took about 4ns after the last comparator to settle. An improvement to the current mirror can substantially improve the performance of folding amplifiers. A sinusoidal input of 5MHz was applied to the folding amplifier. The results are shown in Fig. 9. The switching events follow the ideal switch instances within the delays predicted by the pulse test.

To test the scalability of the design we scaled it up to N = 8 with the same fold size ($I_F = 4\mu A$). The full scale value is now $32\mu A$. The mirrors become slower as the number of output branches increases. The settling time for the full scale rising and falling pulses increase $8.4ns$ and $3.5ns$ respectively.

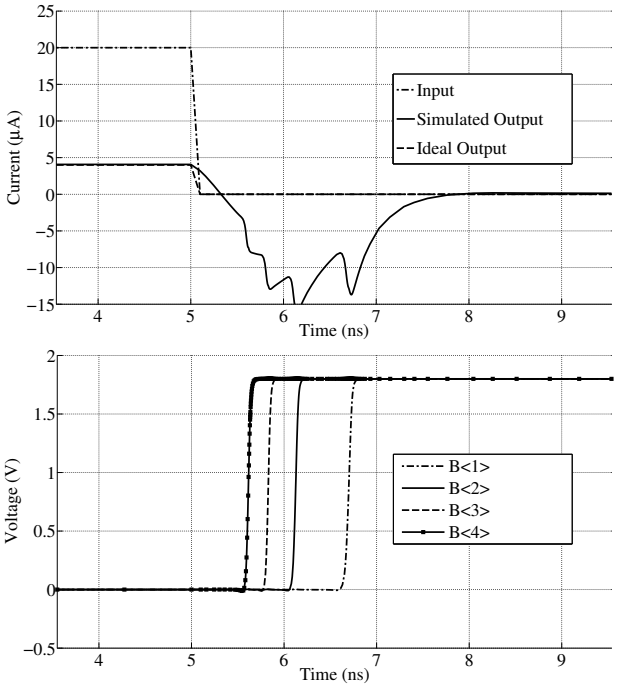

Figure 8. Transient Response for a Full Scale Falling Pulse

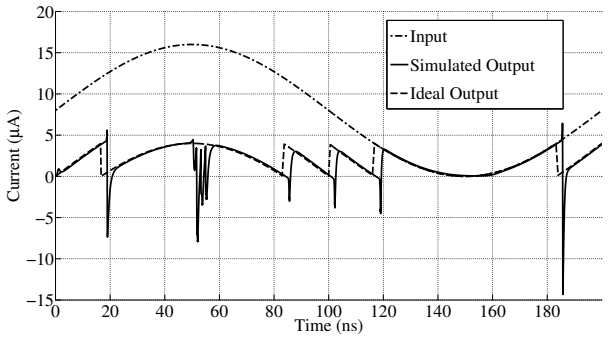

Figure 9. Response to a sinusoidal signal of frequency 5MHz

4. Conclusion

In this paper we presented a minimal current mirror count folding amplifier. Only one current mirror separates the input and output. Comparators were used to decide the switching points of the amplifier. Compared to previous works, the presented amplifier provides a four times faster full-scale response. Such folding amplifier can be very useful for the design of high speed ADC. Improvement in current mirror settling time can substantially improve the performance of current mode folding amplifiers.

5. Acknowledgment

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6. References

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