Implementation of Differential Power Processing Concept to Switched-Capacitor Topology for PV Sub-module Level Power Balancing

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Abstract

Non-convex power characteristic curve with decreased peak power and with multiple local maxima occurs because of the partial shading and mismatching conditions among the series connected modules/sub-modules/cells. A number of power electronics topology has been proposed to equalize voltage of each series connected sub-module while providing an extra current path circuitry for mismatch current. The equalization is done by energy transfer between the sub-modules which brings all sub-modules to the same operating voltage and this collective operation produces a convex output power curve with increased peak power. A power electronics solution including minimum number of components and having higher efficiency is essential in this type of application from the perspective of installation costs and overall efficiency. This paper realizes a differential power processing (DPP) version of the recently presented sub-module level power balancing topology which uses nearly half of the converter number in comparison to the related literature. The DPP version of the topology provides improvement in efficiency for matched conditions and for some arbitrary partial shading patterns conditions over the string. PSpice simulation results are provided to show advantage of the approach in comparison to single output version.

1. Introduction

Since high voltage inverters have high efficiency, the photovoltaic modules are connected in series in order to obtain large voltages [1]. The recent research efforts and technologic developments chronologically introduced us with the central inverters, string inverters, string inverters with multiple inputs allowing independent MPPT at each input, multi-level inverters, micro-inverters for each PV module, DC-DC optimizers at module level, DC-DC optimizers at sub-module level and lastly cell-level MPPT using diffusion charge redistribution (DCR) concept proposed in [2]-[4] which can be used in 'Future Smart PV Modules'. The idea of each approach has arisen as a solution to the partial shading and the mismatch losses with increased granularity [5]. Partial shading and mismatch conditions among the series connected modules/sub-modules/cells suffer from non-convex output power characteristic curve with multiple local maxima and decreased peak power for the whole string/module, including by-pass diodes. This limits the power extraction from the whole string/module [6].

By-pass diodes are connected in parallel with the sub-modules in order to by-pass the sub-modules subjected to partial shading and prevent them to act as a load to the un-shaded modules. When the by-pass diodes are activated due to the shading, the power produced by the by-passed sub-modules is wasted. Consequently, recent researches have concentrated upon re-gaining the by-passed power due to use of by-pass diodes and bringing them to the same operating voltage [6]. Reference [7] benefiting from distributed power electronics concept have proposed synchronous buck converter which is implemented in parallel with sub-module; by employing both inductive and capacitive elements and processing the whole power produced from the sub-module. This topology does not use differential power processing (DPP) concept and overall efficiency highly depends on the converter efficiency. Subsequent studies at sub-module level generally rely on a similar idea which is to transfer energy or redistribute charge between sub-modules using energy storage elements like combination of inductor-capacitor or transformer-capacitor and switches. This energy transfer brings all sub-modules to the same operating voltage and produces a convex output power curve with increased peak power for series connected sub-modules/cells. All these studies process only the power mismatch which is small in comparison to the string power and result in minimum loss. If the sub modules are in balance, they do not ideally lose power. As a result all of them are categorized in DPP concept [6], [8]-[20]. In [6] a bidirectional buck-boost circuit with current control is proposed to guarantee equal section voltages in a module using active voltage sharing. The closed loop control needs current measurement. In [8]-[9] a DPP converter is implemented as a synchronous buck-boost circuit with voltage measurement feedback. The control strategy is designed to allow each and every DPP converter to track the local MPP of its corresponding sub-module. The control strategy searches for a convenient duty cycle on a two-dimensional surface which maximizes the voltage of the string for a temporarily fixed string current. The string voltage information is required by each DPP converter to realize this strategy. Therefore this requires a communication interface to acquire diagnostic data. A conventional perturb-observe MPPT algorithm working on the central inverter gradually moves the previously fixed string current towards the maximum power point value in a 'slow' loop while the local DPP controllers adjust the duty cycles to maximize the string voltage in a 'fast' loop. This control approach may fail under rapidly changing environmental conditions. Hence sub-module voltage and the string current may never converge to its optimal value. The control complexity also increases. In [10] the PV-to-Bus and PV-to-PV DPP architectures for series string are examined for mismatch conditions using Monte Carlo simulation and compared to series strings with and without bypass diodes. It is stated that the flyback topology can be

employed in the PV-to-bus converter and the buck-boost topology can be employed in the PV-to-PV converter. Their simulation results showed better performance for the PV-to-bus architecture. But the switches used in PV-to-bus converters must be rated to the bus voltage and this results in some disadvantages from the point of view of the application. In [11]-[12] a local control strategy requiring the current and voltage measurements is developed for the bidirectional buck-boost converter employed as a DPP in the PV-to-PV architecture which is proposed by [10]. A basic perturb and observe algorithm running on the local controller tries to maximize the power of each PV element in order to find the corresponding duty cycle. The converter efficiency is reported to be around 96%. In [13] several differential energy conversion architectures and associated local controls have been analyzed. The simulation results showed that the isolated flyback converter employed in a PV-to-bus architecture tends to process the least amount of power. In [14]-[20] another bidirectional flyback converter which allows DPP and its control approach have been analyzed. The secondary ports of the flyback transformers are connected in parallel and disconnected from the module/string output. This solves the disadvantage mentioned in [10] and brings the advantage of using low voltage rated switches and results in a control without need for additional sensing. This architecture increases the string cable usage since it needs dual-core cable at the secondary of the transformer. In [21]-[24] resonant switched-capacitor (SC) converters are configured in a parallel-ladder architecture with strings of PV cells at the sub-module level to improve energy capture in the event of shading or mismatch. The balancing action extends from the sub-module level with added one more converter stage to the entire series string through a dual-core cable and connector. All the above studies generally use both inductive and capacitive elements together and employ number of *2n* or *2n-1* converters to prevent mismatch losses of number of *2n* sub-modules which result in increased cost and power electronics losses.

The recently proposed topology [26] benefits from SC converter concept in a different manner than the similar publication available in the literature [21]-[24] and actually is an application of [2]-[4] with some novelties such as sub-module level power balancing, stopping the switching in absence of shading, string level extension, and reduced number of power electronics components as compared to the related published literature listed in the reference section. Sub-modules are configured in parallel-ladder architecture to form a string as shown in Fig. 1. These sub-modules which are supported by a charge storage capacitor are switched with each other in order to equalize voltage of each series connected sub-module while providing an extra current path circuitry for mismatch current. The collective operation produces a convex output power curve with increased peak power. A power electronics solution including minimum number of component and having higher efficiency is essential in this type application from the perspective of installation costs and overall efficiency. The recently presented sub-module level power balancing topology in [26] uses nearly half of the converter number in comparison to the literature. This leads to the reduced power electronics losses, less cost and volume of the converter circuit.

This paper focuses on improving the overall efficiency at the sub-module level by applying the differential power processing concept proposed by [3]. The dual output version of the topology which allows DPP provides improvement in efficiency for matched conditions and for some arbitrary partial shading patterns conditions over the string. PSpice simulation results are provided to show advantage of the approach in comparison to single output version.

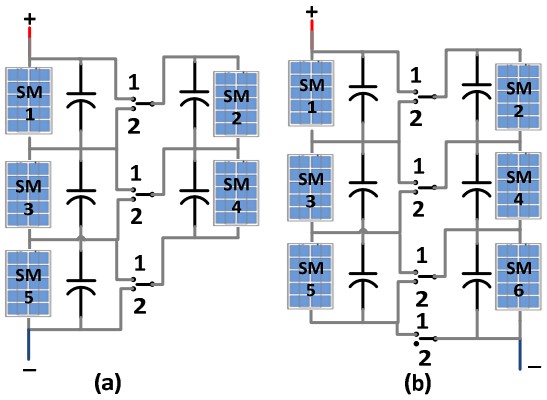

Fig. 1. Recently proposed single output version of the ladder configured switched-sub module topology [26]

2. Disadvantage of the Single Output Configuration

The single output version of the capacitor supported switched sub-module architecture was the first ladder-type configured SC converter topology for sub-module level power balancing [26]. The topology requires *n* capacitors and *n+1* switches for number of *n* sub-modules while traditionally configured SC converters require *2n-1* capacitors and *2n* switches.

A single output version of this topology shown in Fig. 1a requires continuous switching. This causes an insertion loss even if there is no partial shading and mismatch among the sub-modules, because the power produced by switched-ladder string shown on the right in Fig. 1a must be processed in order to transfer this power to the load side. Hence the whole power produced by the switched ladder string is lost when switching is stopped [3], [5]. The topology shown in Fig. 1b allows stopping the switching process in position 1 while partial shading is not present and this results in reduced insertion loss. Stopping the switching may be a good solution under uniform irradiation conditions for the PV modules whose characteristics perfectly match. It requires detection of the partial shading and hence communication interfaces between PV modules.

The loss mechanism in SC converter has two components; slow switching limit (SSL) and fast switching limit (FSL) losses. For the single output topology shown in Fig. 1b, the percentage insertion losses for the SSL and FSL were derived following the basics of the switched capacitor converter and given in (1) and (2) [26].

$$IL_{SSL} = \frac{I_{MP}}{4N\,V_{MP}\,C\,f_{sw}\,(2N+1)^2}\left[\sum_{i=1}^{N}(2i-1)^2\right] \qquad (1)$$

$$IL_{FSL} = \frac{2\,R_{eff}\,I_{MP}(2N-3)}{V_{MP}\,N\,(2N+1)} \qquad (2)$$

where I_{MP} and V_{MP} is the maximum power current and maximum power voltage of the sub-module respectively, C is the capacitance value of capacitor connected in parallel to sub-module, f_{sw} is the switching frequency, N is the number of sub-module connected in one arm of the proposed topology, R_{eff} effective resistance of the switch on-resistance in series with any

interconnect resistance. The FSL losses highly depend on the N and R_{eff} while the SSL losses highly depend on the capacitance and the switching frequency.

As an illustration for the switched sub-modules string with the following parameters N of 3, maximum power voltage of 11.28 V, maximum power current of 4.66 A under 100% irradiation and the capacitor value of 20 µF, the switching frequency of 50 kHz, and switch on-resistance of 10 mΩ, the SSL insertion loss is calculated as 2.5% from (1), the FSL insertion loss is calculated as 0.12% from (2). The total insertion loss is calculated as the square root of quadratic sum of these two components and calculated as 2.5% for the perfectly matched condition

The capacitance size C and switching frequency f_{sw} can be chosen such that the SSL insertion loss meets design requirements. They can also be determined by plotting the output current versus frequency and capacitance value as shown in Fig. 2. The average output current transferred by one switched capacitor is given by (3). For the sub-module with the characteristic of 2.33 A maximum power current and 11.49 V maximum power voltage under 50% irradiation (50% partial shading case is chosen); the capacitance must transfer average current of $(I_{M100}- I_{M50})/2$=1.16 A at the voltage difference (V_1-V_2) of 0.21 V.

$$I = Cf_{sw}(V_1 - V_2)\left(\frac{1 - e^{-\frac{1}{2f_{sw}R_{eff}C}}}{1 + e^{-\frac{1}{2f_{sw}R_{eff}C}}}\right) \qquad (3)$$

According to the analysis and Fig. 2, the most convenient value of the capacitance-frequency pair corresponds to the point on the 1.16 A plane which is most closest to the origin.

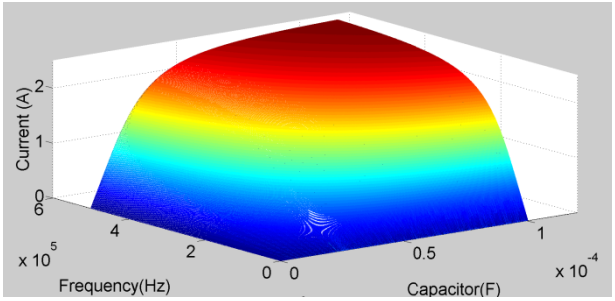

Fig. 2. Output current versus frequency and capacitance

The SSL loss generally outweighs and may be undesirable from the point of view of the application since it is a permanent loss in absence of shading. A more comprehensive solution, which in addition to the stopping the switching, is needed in order to prevent the insertion losses. The dual-output configuration proposed by [2] can also be adapted to the switched sub-module level power balancing topology proposed by [26].

3. Dual Output Configuration – DPP

The dual output configuration of the proposed topology allows differential power processing which loses a small amount of power by only processing the mismatch power among the sub-modules. As a consequence overall efficiency is increased.

For the DPP, the outputs of the two-arm strings are simply disconnected from each other and the available power on the string is directly extracted from the both string arms. As a result no power is processed through the switching circuitry in order to extract this power to the load side since all sub-modules are in balance for the matched condition [2]. Dual output version of the switched sub-module architecture is shown in Fig. 3.

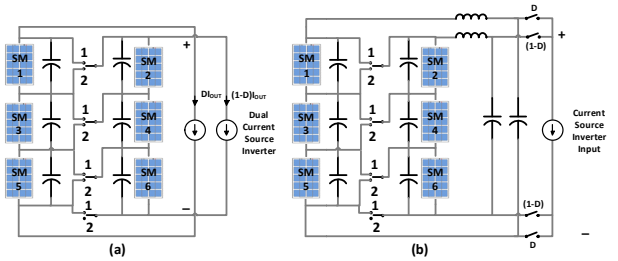

Fig. 3. Dual output version of the switched sub-module topology

For the matched or the symmetric partial shading condition over the two arms, the duty cycle (D) of the dual current input interface is adjusted such that the equal amount of current must be drawn from both arms. This means D=0.5. D is adjusted such that the ratio of the currents drawn from the both arms matches with the partial shading ratio of the shaded side in comparison to the non-shaded side. As an example case, it is assumed that the left-hand side string is exposed to 1 sun while the right-hand side string is exposed to 0.4 sun because of 60% partial shading. Hence the duty ratio (D) of the left-hand side string must be adjusted to draw 1 unit current while the duty ratio (1-D) of the right-hand side string must be adjusted to draw 0.4 unit current to minimize the processed power through the switches. This means D=(1/1+0.4)≈0.71 [2].

4. Simulation Results

The subsequent simulations have been done in PSpice. The sub-module is modeled using the one diode model of the PV element. Following parameters are used in the simulation; maximum power voltage of 11.2 V, maximum power current of 4.66 A under STC, parallel resistance of 75.36 Ω, series resistance of 0.326 Ω, capacitor of 20 µF, switching frequency of 50 kHz, and the switch on-resistance of 10 mΩ are used in the switched sub-module converter circuit. An example string with 6 sub-modules which are configured in 3//3 ladder-type architecture is simulated to show that improvement in efficiency for matched condition and for some arbitrary partial shading patterns over the string can be achieved.

Fig. 4 shows the power versus voltage curves under uniform irradiation for three different cases; 6-series string, 3//3 single output, 3//3 dual output. Fig. 5 shows the P-V curves for partial shading condition; 3 sub-modules on the right-hand side is 50% shaded and overall shading is 25%. The results are concluded in Table 1 showing the maximum powers and efficiencies. For the uniform irradiation, the dual output has the conversion efficiency of 100% while the single output version has the conversion efficiency of 97.4% which proves the loss analysis with a power loss value of 2.5%. This result shows the superior performance of the dual output version over the single output version under uniform irradiation condition. For the aforementioned partial shading case, the dual output has the conversion efficiency of 74.83% while the single output version has the conversion efficiency of 72.44%.

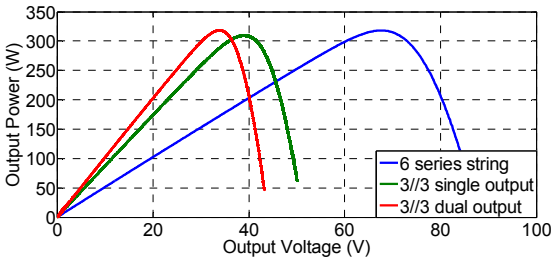

Fig. 4. Simulation results under uniform irradiation

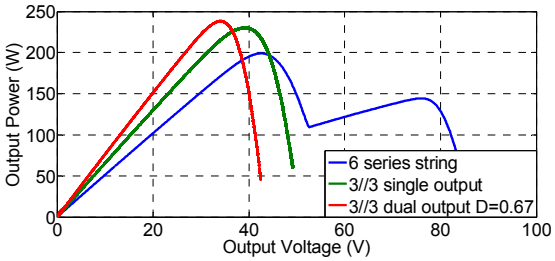

Fig. 5. Simulation results under 25% partial shading

Table 1. Comparison of maximum powers and efficiencies

Configuration	Uniform irradiation		%25 overall eff. (RHS. 50% shaded)	
	Power (W)	Conv. Eff. %	Power (W)	Conv. Eff. %
6 series + by-pass diode	318.06	100	173.87	54.66
3//3 single output	309.83	97.4	230.42	72.44
3//3 dual output	318.06	100 D=0.5	238.03	74.83 D=0.67

6. Conclusion

This paper focuses on improving the overall efficiency at the sub-module level by applying the DPP concept proposed by [3]. The dual output version of the topology which allows DPP provides improvement in efficiency for matched conditions and for some arbitrary partial shading patterns conditions over the string. PSpice simulation results are provided to show the advantage of the approach in comparison to the single output version.

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