An Attempt to Improve Output Voltage Quality of Developed Multi-Level Inverter Topology by Increasing the Number of Levels

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Abstract

In this paper, an improved Cascaded Multi-Level Inverter (CMLI) topology which can be "symmetric" or "asymmetric" is proposed. The improved topology can produce higher number of levels using lower number of components. Higher number of levels leads to generation of a high quality with low Total Harmonic Distortion (THD) output voltage waveform. To increase number of voltage levels, two algorithms are proposed for determination of magnitude of dc voltage sources, which are investigated and the most effective one is introduced. To verify operation of proposed topology, it is modeled and simulated in PSCAD/EMTDC software. Proper performance of proposed topology is confirmed by obtained simulation results.

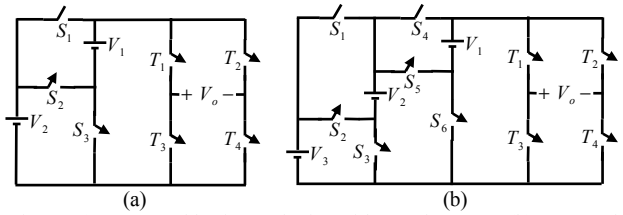
Keywords—cascaded multi-level inverter; symmetric and asymmetric topology; number of level; number of component

1. Introduction

In recent years, brilliant properties of Multi-Level Inverters (MLIs) such as; capability of operation in high power and medium voltage, low voltage stress on switches, generating a nearly sinusoidal voltage waveform with high power quality and low THD, have introduced them as good alternative for conventional two (three) level inverters, in industrial applications [1-4]. The operation of MLIs is based on the synthesizing of several small dc voltage sources to achieve a staircase voltage waveform. In general, the MLIs can be classified into three main categories: Diode-Clamped Multi-Level Inverters (DCMLIs), Flaying Capacitor Multi-Level Inverters (FCMLIs) and Cascaded Multi-Level Inverters (CMLIs) [5-8]. In DCMLIs, the output voltage wave form is achieved by summing up the voltage of series connected capacitors. Higher number of needed capacitors and diodes, for generating of higher number of output voltage levels, is the main disadvantage of this family. FCMLIs have a nearly same operational concept with DCMLIs. The combination of voltage of flying capacitors, form the output voltage waveform. Again, higher number of required flying capacitors to produce higher number of levels, is the main drawback of FCMLIs. The CMLIs are considered to have simplest structure and operation concept, among above mentioned MLIs. In this family, the output voltage is obtained by combination of output of several cascaded basic units. Simple structure and simple control strategy are the main benefits of CMLIs. On the other hand, large number of switches, gate driver circuits and dc sources, are the main disadvantages of the CMLIs, which leads to a bulky and costly topology. So, there is need to proposed new topologies that use minimum number of components. In [9] a new CMLI based on transformer is presented, which uses minimum number of switches and gate driver circuits. On the other hand, due to the application of transformer, the topology is bulky and heavy. Cascaded H-Bridge (CHB) based MLI, with several algorithms for deciding about the magnitude of dc sources, is presented in [10-12]. A 7-level CMLI has been presented In [13]. In this paper, we have developed the 7-level topology presented in [13] and proposed a general multi-level inverter topology. In the proposed topology, number of levels have been greatly increased. For example, by adding only two switches to the presented 7-level inverter, the number of levels are doubled plus one. In the following, the proposed topology is introduced. Symmetric and asymmetric version of proposed topology is investigated. Comparison comes in the third section. Section four contains simulation results. Finally the conclusion comes at the fifth section.

2. Proposed Topology

The basic form of proposed Cascaded Multilevel Inverter (CMLI) is illustrated in Fig. 1a. The basic topology is comprised of two dc sources and 6 unidirectional and one bidirectional switches. Unidirectional Switches are composed of one IGBT and one antiparallel diode, while bidirectional ones include two IGBTs and two diodes. It must be noted that 4 of these switches belong to the applied H-bridge for producing negative voltage levels. If the magnitude of dc sources are considered to be the same, the proposed basic topology will be symmetric, else it will be asymmetric. The proposed symmetric basic topology can produce 5 output voltage levels, but this amount can be increased for asymmetric topologies. Maximum number of levels that this basic topology can produce is 7, for example, if the magnitude of V_1 and V_2 dc sources are considered to be 10V and 20V, respectively, the topology can produce 7 levels.



(a) (b)

Fig. 1. (a) Proposed basic topologies with two dc sorces; (b) Proposed topology with three dc sources

If the basic topology is extended, a new topology is proposed (Fig. 1b) which is composed of three dc sources and 8 unidirectional and 2 bidirectional switches. This new topology in its symmetric form, can generate 7 output voltage levels. As mentioned before, number of levels can be increased for asymmetric versions, for instance, for $V_1 = 10V$, $V_2 = 20V$ and $V_3 = 40V$, 15 output levels can be achieved . Switching pattern of proposed topology for this condition is illustrated in Table I.

TABLE I. SWITCHING PATTERN OF PROPOSED 15 LEVEL INVERTER

No.	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	V_o
1	0	0	0	0	0	0	1	1	0	0	0
2	0	0	0	0	0	0	0	0	1	1	0
3	0	0	0	0	0	1	1	0	0	1	10
4	0	0	1	1	0	0	1	0	0	1	20
5	0	0	1	0	1	0	1	0	0	1	30
6	1	0	0	1	0	0	1	0	0	1	40
7	1	0	0	0	1	0	1	0	0	1	50
8	0	1	0	1	0	0	1	0	0	1	60
9	0	1	0	0	1	0	1	0	0	1	70
10	0	0	0	0	0	1	0	1	1	0	-10
11	0	0	1	1	0	0	0	1	1	0	-20
12	0	0	1	0	1	0	0	1	1	0	-30
13	1	0	0	1	0	0	0	1	1	0	-40
14	1	0	0	0	1	0	0	1	1	0	-50
15	0	1	0	1	0	0	0	1	1	0	-60
16	0	1	0	0	1	0	0	1	1	0	-70

It must be noted that 1 and 0 represents the on and off states of the switch. If we keep on extending the proposed basic topology, the new general topology can be proposed for the CMLIs which is depicted in Fig. 2.

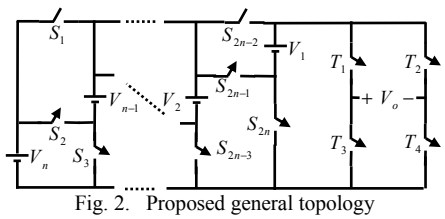


Fig. 2. Proposed general topology

The general topology include n dc sources and $3n+1$ switches. Depended on the values of dc sources, the proposed general topology can be symmetric or asymmetric. In the following, the symmetric and asymmetric versions of proposed general topology are investigated.

2.1. Proposed Symmetric General Topology

In symmetric topology it is assumed that magnitude of all dc sources are the same and equal to V_{dc} . If n dc sources are used, the proposed symmetric topology is be able to produce $2n+1$ voltage levels at the output.

$$N_{level} = 2n + 1 \quad (1)$$

$$N_{Source} = n \quad (2)$$

$$N_{Switch} = 3n + 1 \quad (3)$$

Since all dc sources have the same values, the variety number of dc sources is equal to one, which reduces the total cost of inverter.

$$N_{Variety} = 1 \quad (4)$$

To calculate standing voltage of the proposed topology, it is enough to sum up standing voltages of all switches. Maximum amount of voltage that S_i , $(i = 1,2,\cdots,3n-2)$ and T_j , $(j = 1,2,3,4)$ switches should withstand are V_{dc} and nV_{dc} , respectively. So we have:

$$V_{standing} = (7n - 3)V_{dc} \quad (5)$$

2.2. Proposed Asymmetric General Topology

To increase number of generated voltage levels and improve the quality of produced voltage waveform, asymmetric topologies are preferred to symmetric ones. In the proposed asymmetric topology, two algorithms are proposed for determination of magnitude of dc sources, which are described in the following:

1) First algorithm

In this algorithm it is assumed that the magnitude of first dc source is V_{dc} and the remaining ones have the magnitude of ($V_1 = V_{dc}$, $V_i = 2V_{dc}$ *for* $i = 2,3,\cdots,n$). This algorithm enables the topology to produce $4n-1$ voltage levels at the output. It must be noted that all the odd and even voltage levels can be produced by this algorithm (n represents the number of dc sources.).

$$N_{level} = 4n - 1 \quad (6)$$

$$N_{Source} = n \quad (7)$$

$$N_{Variety} = 2 \quad (8)$$

$$V_{standing} = (14n - 11)V_{dc} \quad (9)$$

2) Second algorithm

In second algorithm, the relationship between magnitudes of dc sources is assumed to be as follows:

$$V_i = 2^{(i-1)}V_{dc} \quad for \quad i = 1,2,\cdots,n \quad (10)$$

If this algorithm is applied for deciding about the values of dc sources, the topology will be capable of producing $2^{(n+1)}-1$ (odd and even) voltage levels at the output.

$$N_{level} = 2^{(n+1)} - 1 \quad (11)$$

$$N_{Source} = n \quad (12)$$

$$N_{Variety} = n \quad (13)$$

$$V_{standing} = \left[(12)2^{(n-1)} - 9\right]V_{dc} \quad (14)$$

3. Comparison

To investigate benefits and drawbacks of the proposed inverter, it should be compared with previously presented CMLI topologies. The proposed topology is compared with symmetric and asymmetric Cascaded H-Bridge (CHB) topology, presented in [10-12]. In this paper the symmetric CHB topology is referred to as R_1. The asymmetric CHB topology, in which the magnitude of dc sources are decided based on binary order ($V_i = 2^{(i-1)}V_{dc}$ *for* $i = 1,2,\cdots,n$) is indicated by R_2. Also the topology presented in [13] which is a 7 level inverter has been selected for comparison that is shown by R_3. To make a better comparison, R_3 has been extended to be a Multi-

Level Inverter (like Fig. 3b), in which the value of dc sources are determined based on a geometric progression by a factor of two ($V_i = 2^{(i-1)}V_{dc}$ *for* $i = 1,2,\cdots,n$). Also the proposed symmetric topology is displayed by P_1, the proposed asymmetric topology applying first and second algorithms for deciding about the magnitude of dc sources are shown by P_2 and P_3, respectively.

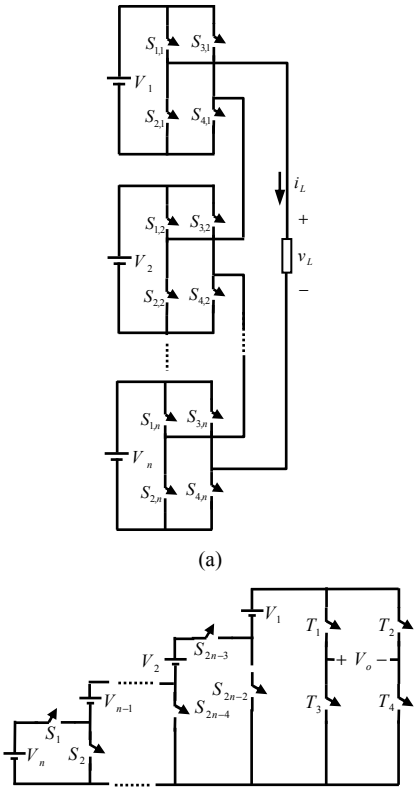


Fig. 3. Topologies selected for comparison

Four important factors have been selected for comparison; number of generated levels, number of switches, number of dc sources and maximum output voltage. The standing voltage on the switches is not considered in this study. Brief description of selected topologies for comparison, is shown in Table II.

TABLE II. DESCRIPTION OF SELECTED TOPOLOGIES FOR COMPARISON

Topology	Number of sources	Number of switches	Number of Levels	Maximum output voltage
P_1	n	$3n+1$	$2n+1$	nV_{dc}
P_2	n	$3n+1$	$4n-1$	$(2n-1)V_{dc}$
P_3	n	$3n+1$	$2^{n+1}-1$	$(2^n-1)V_{dc}$
R_1	n	$4n$	$2n+1$	nV_{dc}
R_2	n	$4n$	$2^{n+1}-1$	$(2^n-1)V_{dc}$
R_3	n	$2n+2$	$2n+1$	$(2^n-1)V_{dc}$

Fig. 4 shows the relationship between number of levels and number of switches.

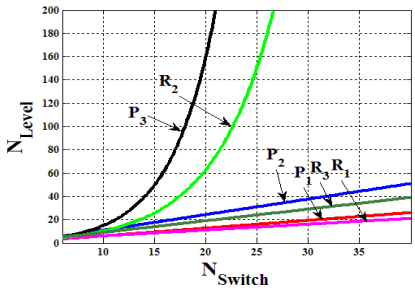


Fig. 4. Number of levels vs. number of switches

According to Fig. 4, the proposed P_3 topology generates higher number of levels for a given number of switches, compared with other topologies. Due to the higher number of produced levels, the quality of output voltage waveform is high and the Total Harmonic Distortion (THD) is small. From other point of view, it is seen that the proposed P_3 topology uses minimum number of switches for producing a specified number of voltage levels, which leads to a reduction in size, losses and cost of inverter. Relationship between number of levels and number of dc sources is illustrated in Fig. 5 for different topologies.

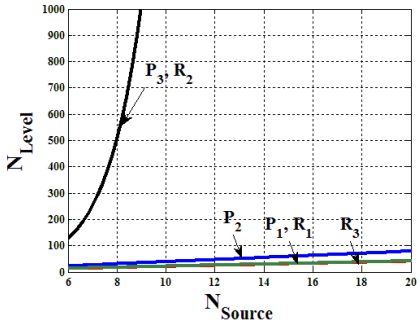


Fig. 5. Number of levels vs. number of sources

Fig. 5 shows that for a given number of dc sources, the proposed P_3 and R_2 topologies produce higher number of levels in comparison with other topologies. Also it can be concluded that for generating a given number of levels at the output, the proposed P_3 topology uses minimum number of dc sources. This fact reduces the size and cost of inverter.

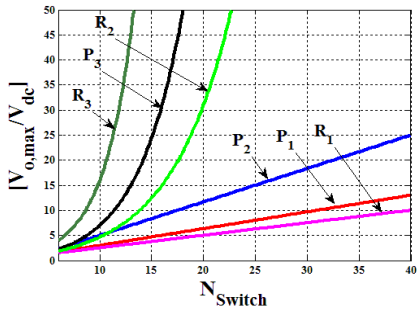


Fig. 6. Normalized maximum output voltage vs. number of switches

The relationship between maximum output voltage and number of switches and dc sources are displayed in Fig. 6 and 7. It can be seen from Fig. 6 that the R_3 topology can produce higher values of maximum output voltage for a given number of switches in

comparison with other topologies. From this point of view, the proposed P_3 topology is in second place. According to Fig. 7, the proposed P_3 topology besides R_2 and R_3 topologies, apply minimum number of dc sources to produce a defined value of maximum output voltage. Using minimum number of dc sources decreases the size and cost of inverter.

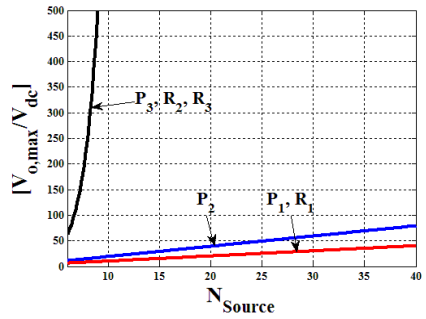


Fig. 7. Normalized maximum output voltage vs. number of sources

Comparison results introduces the proposed P_3 topology as the most efficient one among selected topologies, since it uses minimum number of switches and dc sources for producing a defined number of output voltage levels, in comparison with other selected topologies. This property reduces the inverter total losses, size and cost. On the other hand, the P_3 topology can produce maximum number of voltage levels by means of a given number of switches and dc sources, compares with other topologies. So, the output voltage waveform has high quality and low THD. Also, this topology can generate maximum value of maximum output voltage, by using a specified number of dc sources, which is very suitable for high power applications. It is worthy to note that, in asymmetric topologies, there is always an increase in inverter cost due to the high variety number of dc sources. The more the variety number of dc sources, the high the cost increment of the inverter. Low variety number of dc sources and low voltage stress on the switches, beside the simple the structure, are the main advantages of symmetric topologies.

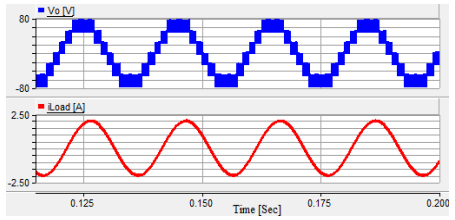
4. Simulation and Experimental Results

In this section, the proposed topology with two and three dc sources are selected to be modeled and simulated in PSCAD/EMTDC software, to verify performance of proposed topology. Experimental results of proposed topology with two input dc sources has also been presented. The Sinusoidal Pulse Width Modulation (SPWM) technique is applied for switching of the inverter, where the frequency of carrier and reference waveforms are 5 kHz and 50 Hz, respectively. During the simulations, the modulation index is considered to be 0.9. A resistive-inductive load with $R = 30\Omega$ and $L = 50\,mH$ is considered as the load. Information used during simulations have been summarized in Table III.

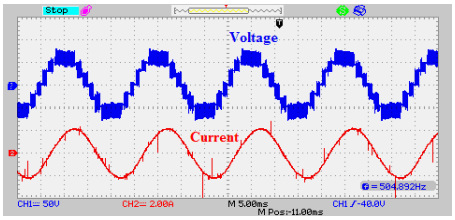
TABLE III. VALUES OF PARAMETERS USED IN THE SIMULATIONS

Parameter	Symbol	Value	Unit
Fundamental frequency	f	50	Hz
Switching frequency	f_{sw}	5000	Hz
Modulation index	m	0.9	-
Load resistance	R	30	Ω
Load inductance	L	50	mH

Fig. 8a shows the output voltage and current waveforms of the proposed topology with two input dc sources (shown in Fig. 1a), where $V_1 = 25V$ and $V_2 = 50V$. It is seen that the output voltage waveform is composed of 7 levels. Maximum output voltage is $75V$ and the peak value of the load current is about $2A$. The THD of the output voltage is about 19%. Fig. 8b shows the experimental results for load voltage and current waveforms of proposed topology with two dc sources. As seen, the experimental results are in good accordance with simulation results.



(a)



(b)

Fig. 8. (a) Simulation; and (b) Experimental; results obtained for load voltage and current waveforms of proposed two input dc source topology with $V_1 = 25V$ and $V_2 = 50V$

Fig. 9a shows the voltage and current waveforms of the load for proposed symmetric topology (P_1), while the magnitude of all three dc sources are considered to be $20V$. The measured THD of load voltage in this case, is equal to 19.99% which is acceptable. This amount can be reduced by application of an output filter. As it can be seen, 7 voltage levels have been produced at the output. Also, maximum output voltage on the load is $60V$. Due to the considerable value of the load inductance, generated load current is almost a sinusoidal waveform with peak value of $1.6A$. The output voltage and current waveforms of proposed topology with three dc sources, applying first algorithm for determination of magnitude of dc sources (P_2), are shown in Fig. 9b. In this scenario, the magnitude of V_1, V_2 and V_3 dc sources are assumed to be $10V$, $20V$ and $20V$, respectively. As seen from Fig. 9b, an 11 level voltage waveform with peak value of $50V$ has been produced at the output. The THD of voltage waveform is equal to 11.64%. The load current is a sinusoidal waveform with magnitude of $1.33A$. Fig. 9c shows the load voltage and current waveforms of proposed asymmetric topology with three dc sources and applying second algorithm for deciding about values of dc source ($V_1 = 10V$, $V_2 = 20V$, $V_3 = 40V$). As this figure indicates, a 15 level load voltage with peak value of $70V$ has been produced. THD of the output voltage for this case is equal to 7.95%. Also a sinusoidal waveform with maximum value of $1.86A$ is observed for load current. Simulation results show that if second algorithm is applied for determination of magnitude of dc sources, maximum output voltage and number of levels will increase, quality of produced voltage waveform will be improved and its THD will decrease. It is also seen that the proposed topology can operate properly for any kind of loads, including inductive loads with low power factor. Produced load

current is an almost sinusoidal waveform with high quality and low THD, which is highly desired.

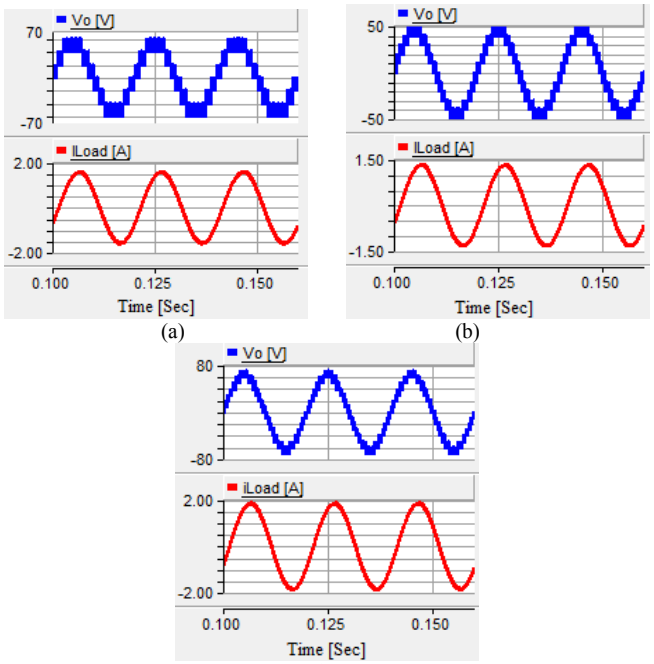


Fig. 9. Load voltage and current waveforms for proposed (a) symmetric topology; (b) asymmetric topology applying first algorithm; (c) asymmetric topology applying second algorithm; with three dc sources

5. Conclusion

In this paper, a new topology is proposed for cascaded multi-level inverters. The proposed topology can be symmetric or asymmetric. In symmetric topology, the variety number of applied dc sources is only one, so the total cost of inverter decreases. The voltage stress is considerably low in symmetric topologies in comparison with asymmetric ones, so it is possible to use switches with low rating values, which are much smaller and cheaper. On the other hand, asymmetric topologies produce higher number of voltage levels which leads to generation of higher quality and low THD output voltage waveform. To increase the number of voltage levels and maximum output voltage, two algorithms are proposed for deciding about the values of dc sources. To evaluate the advantages and disadvantage, the proposed topology is compared with two previously presented cascaded multi-level inverters. The benefits of proposed topology are confirmed by comparisons. The proposed topology with two and three dc sources are modeled and simulated in PSCAD/EMTDC to verify the performance of proposed structure. The proposed topology with two input dc sources is also implemented practically. The obtained experimental and simulation results validate the proposed topology and theoretical concepts.

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