Reduction of coupling capacitance, using a capacitor-transistor coupling circuit

Majid Eslami Farsani [1], Noushin Ghaderi [2]

[1] Faculty of Engineering, Shahrekord University, Shahrekord, Iran, 88186/34141
majid.eslami@stu.sku.ac.ir
[2] Faculty of Engineering, Shahrekord University, Shahrekord, Iran, 88186/34141
ghaderi.nooshin@eng.sku.ac.ir

Abstract

In this paper, a new coupling circuit is presented. This circuit uses a new method of subthreshold region biasing to decrease the value of coupling capacitor. In proposed circuit the Coupling capacitor is decreased about 98% in comparison with the ordinary capacitive coupling circuit. In addition, the proposed coupling circuit achieves higher linearity. The performance evaluation of proposed circuit is carried out using HSPICE simulations, 180nm technology and 1.8v power supply.

1. Introduction

In analog designs, two circuits with different common mode DC voltages can be connected together through a coupling capacitor. Therefore, the ac signal from the first stage can pass toward the next stage while DC is blocked. However, using the capacitive coupling method degrades the low frequency behavior of the circuit. The combination of the input impedance and the coupling capacitor acts as a high pass filter. For suitable low frequency response, the coupling capacitance must be chosen high enough.

Coupling capacitors are implemented in feedback amplifiers as well. A positive feedback diagram is shown in figure 1. One challenge of positive feedback amplifiers designing is increasing amplifier linearity [1]. Designing of the feedback system (A2) strongly depends on the input and output common mode voltages (Vo' and Vi') of A2. Designing of A2, using the forced DC voltage from the feed forward network, will cause degrading the performance of this system. For example a high input common mode level results in decreasing transistors size of A2 amplifier. It means that the threshold voltage mismatch and nonlinearity will be increased [2]. Capacitor coupling in positive or negative feedback amplifiers remove limited DC voltages in A2 amplifier designing. The coupling capacitors are also used to improve the slew rate of an amplifier [3].

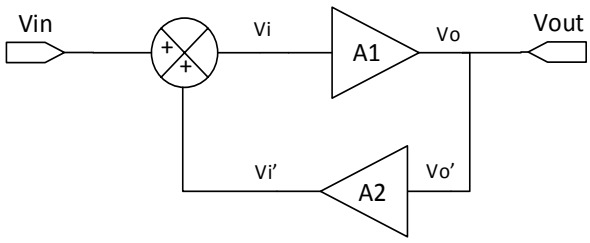


Fig. 1. Positive feedback diagram

This paper is organized as follows. The coupling circuit operation is introduced in section2. In section 3, the proposed circuit is explained and its equations are demonstrated. Simulation results are indicated in section4. Finally, Conclusions are discussed in section 5.

2. Coupling Circuits Operation

Coupling circuits include buffer coupling, transformer coupling and capacitive coupling, are used in varies circuits depend on their properties. Adding buffer coupling will add the power consumption and nonlinearity effects of the amplifier. Transformer coupling implementation is not straightforward in chip designing technology. Capacitive coupling, on the other hand, has a good dc isolation. However, adding a capacitor will add capacitor nonlinearity effects in the circuit [4]. Furthermore a large capacitance will occupy a large area in the chip.

Capacitive coupling circuit is shown in Figure 2. The DC level of Vo and Vo' signals are isolated by C_C capacitor. The bias circuit provide common mode input voltage level of A2 amplifier. Small-signal equivalent of capacitive coupling circuit is shown in Figure 2 (b). In this figure R_b is the output resistance of bias circuit and R_i is the amplifier input resistance.

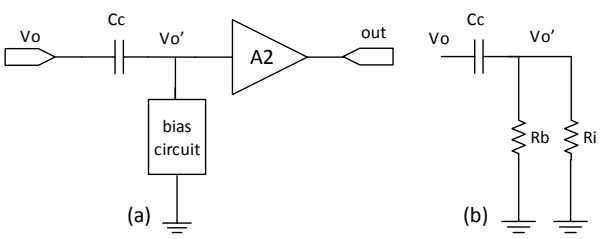


Fig. 2. (a) Capacitive coupling circuit; (b) Small-signal equivalent circuit of capacitive coupling

Capacitive coupling circuit is a high-pass filter which provides a low cut-off frequency (f_c) in the A2 amplifier. This cut-off frequency is calculated as,

$$f_c = \frac{1}{2\pi . c_c (R_b \| R_i)} . \quad (1)$$

Considering that R_i is much larger than R_b, equation 1 will be approximated as,

$$f_c \cong \frac{1}{2\pi . c_c . R_b} . \quad (2)$$

The value of R_b, which depends on the bias circuit, is limited. Therefore, in an ordinary coupling capacitor circuit, the value of f_c strongly depends on the value of C_C. Increasing the value of C_C will decrease f_c. Four typical values of R_b resistance are given in Table 1, for comparison.

Table 1. Output resistance of typically bias circuits

ref	Output impedance (Ω)	Technology
[5]	5.72 k	250nm
[6]	2.1 M	180nm
[7]	266.9 M	90nm
[8]	357 k	180nm

The cut-off frequency of these circuits versus C_C capacitor are plotted in figure 3 using MATLAB software. Increasing the value of R_b, by modifying the bias circuit design, will decrease the value of C_C capacitor.

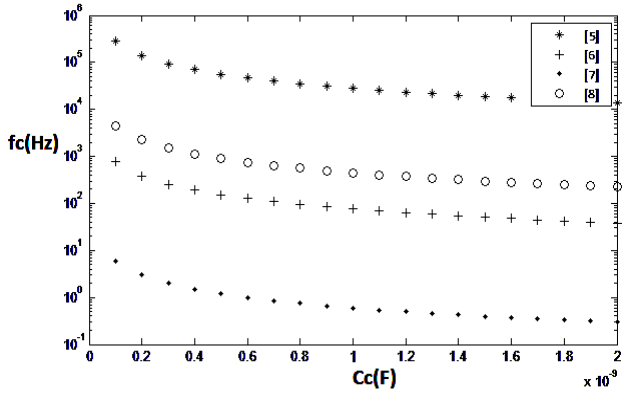


Fig. 3. Cut-off frequency of table 1 circuits versus C_C capacitor

3. Proposed Circuit

Proposed coupling circuit is shown in figure 4 and its Small-signal equivalent circuit is shown in figure 5. The value of Vo'/Vo is obtained as follows,

$$\frac{Vo'}{Vo} = \frac{s.c_c + \frac{1}{r_o}}{s.c_c + \frac{1}{r_o} + gm + \frac{1}{R_i}}. \qquad (3)$$

Equation 3 has one zero as,

$$s_z = -\frac{c_c}{r_o}; \qquad (4)$$

and one pole as,

$$s_p = -c_c.(\frac{1}{r_o} + gm + \frac{1}{R_i}). \qquad (5)$$

If r_o is chosen extremely large, then s_z will be approximately zero. It means that the dc voltage of Vo' and Vo will be isolated completely. For increasing r_o, MC1 transistor is biased in subthreshold region. The value of the drain current of a subthreshold region transistor is [9];

$$Id_{sub} = K.I_0.\exp\left(\frac{V_{GS} - V_{TH}}{\eta.V_T}\right), \; for \; (V_{DS} > 0.1). \qquad (6)$$

Where K is the aspect ratio of transistor (W/L), V_T is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor.

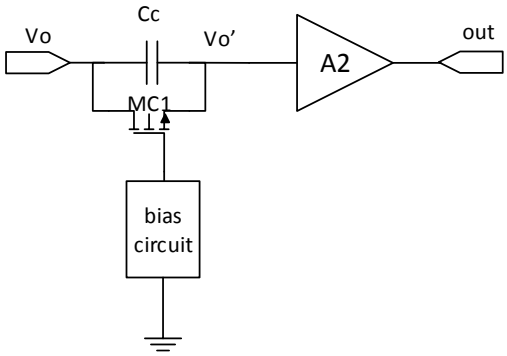


Fig. 4. Proposed coupling circuit

According to the above equation, the value of Id_{sub} is independent of the value of V_{ds}. Considering that r_o is equal to the value of $\partial V_{ds}/\partial Id_{sub}$, r_o will increase considerably. R_i is the input resistance of a CMOS amplifier which is significantly high. Therefore, equation 3 can be approximated as,

$$\frac{Vo'}{Vo} = \frac{s.c_c}{s.c_c + gm}. \qquad (7)$$

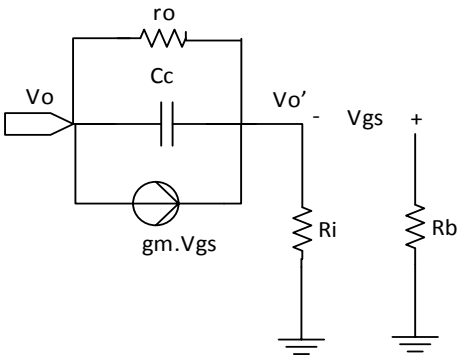


Fig. 5. Small signal equivalent of proposed circuit

According to (7), Proposed coupling circuit isolates the dc voltage of Vo' and Vo by adding a zero at s=0. Cut-off frequency of proposed coupling circuit is calculated as,

$$f_C' = \frac{gm}{2.\pi.c_c}. \qquad (8)$$

The value of trans-conductance (gm) is very low in a subthreshold region transistor (Pico Siemens). Therefore, according to (8) the value of C_C can be chosen very low. The ratio of Cut-off frequency of proposed coupling circuit (f'_C in equation 8) and cut-off frequency of ordinary coupling circuit (f_C in equation 2) is calculated as,

$$\frac{f_C^{'}}{f_C} = gm.R_b \,. \qquad (9)$$

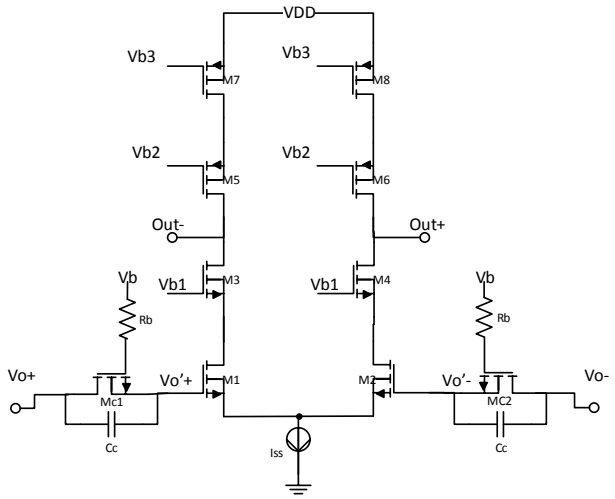


Fig. 6. Proposed circuit which is applied to a telescopic op-amp

According to (9), if the value of R_b is equal to 1/gm, then f'_c will be equal to f_c. For example, if the valve of gm is 1 Pico-Siemens and R_b is 1 tera-ohm then f'_C and f_C will be equal. However, implementation of a tera-ohm resistor is impossible in chip design technology. The proposed coupling circuit is very straightforward to implement. For example, this circuit is applied to a telescopic op-amp, which is shown in figure 6. In this circuit, Vo- and Vo'- are isolated by proposed coupling circuit. The input dc common mode voltages of M1 and M2 is adjusted by adjusting the value of V_b.

4. Simulation results

In this section, simulation results of the proposed coupling circuit are shown and the proposed coupling circuit is compared with the ordinary capacitive coupling circuit. The circuits have been designed in a typical 0.18 µm CMOS process which is applied to the mentioned telescopic op-amp and simulated by HSPICE software. R_b value of proposed coupling is considered as 1k ohm and R_b value of capacitive coupling (figure2) is considered as 1G ohm to achieve the best result in the ordinary circuit.

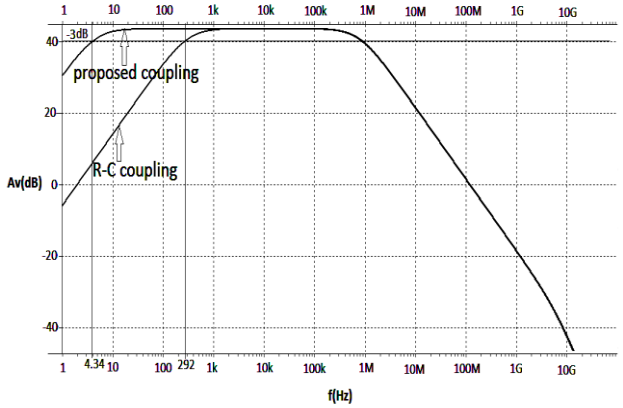


Fig. 7. Ac simulation results of proposed coupling and capacitive coupling

Ac simulation results, using the same value of C_C (=1pF) and C_L (=1pF) for both circuits, are shown in figure 7. The proposed coupling achieves a low cut-off frequency about 4 Hz which is 288 Hz smaller than cut-off frequency of the ordinary capacitive coupling in the same process. To achieve the same cut-off frequency, the coupling capacitor of the ordinary circuit must be increased to the value of 72pF.

Table 2. Output resistance of typically bias circuits

Coupling circuit	R_b (Ω)	C_C	THD (dB)	Low cut-off frequency (Hz)
Proposed coupling	1k	1pF	-65.6	4
Capacitive coupling	1G	1pF	-65.8	292
Capacitive coupling	1G	72pF	-50	4

Monte-Carlo simulation results for 0.5µm variations of the Mc1 and Mc2 widths are used in the proposed coupling circuit which is shown in fig.8.

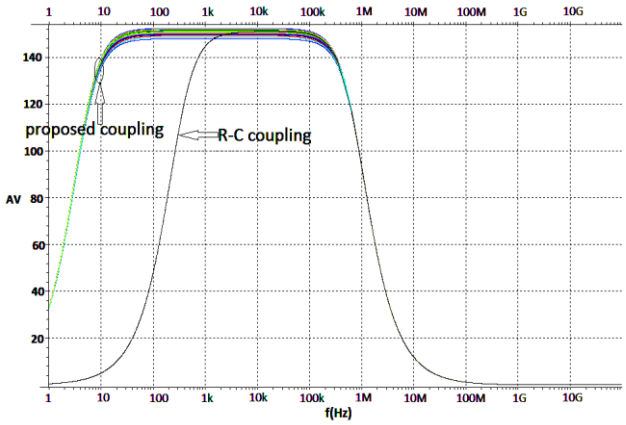
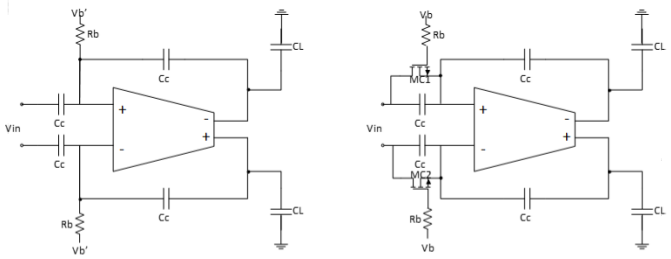


Fig. 8. Monte-Carlo simulation for 0.5 µm variation in width of Mc1 and Mc2 transistors

Closed loop configuration shown in fig.9 is used to study the linearity of the circuits. Fast Fourier Transfer (FFT) result of the proposed coupling and ordinary coupling for a 100 kHz, 1 Vp-p output signal, considering the same bandwidth for two circuits, are shown in figure 10.



(a) (b)

Fig. 9. (a) Capacitive coupling closed loop configuration, (b) proposed coupling closed loop configuration

As demonstrated in figure 10, the harmonic value of proposed coupling are decreased and proposed coupling

achieves higher linearity. Long transient simulation result of the proposed coupling and capacitive coupling for a 100 kHz and .1 V_{p-p} output signal are shown in figure 11.

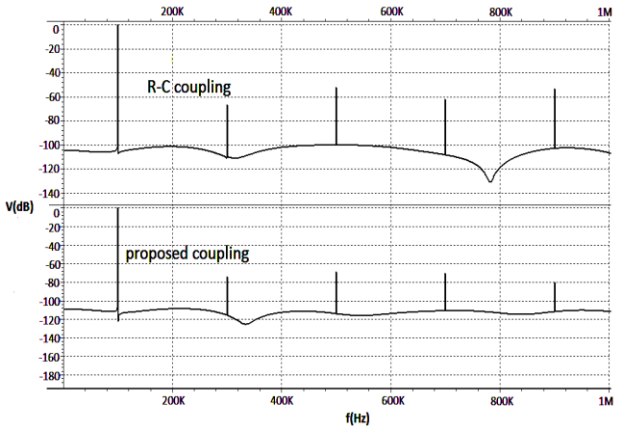


Fig. 10. FFT result of the proposed coupling and capacitive coupling for a 100K Hz and 1 V_{P-P} output signal

As can be seen, the DC value of output signal does not change during the long time simulation. Finally, characteristics of designed coupling circuit are summarized in table 2 for comparison.

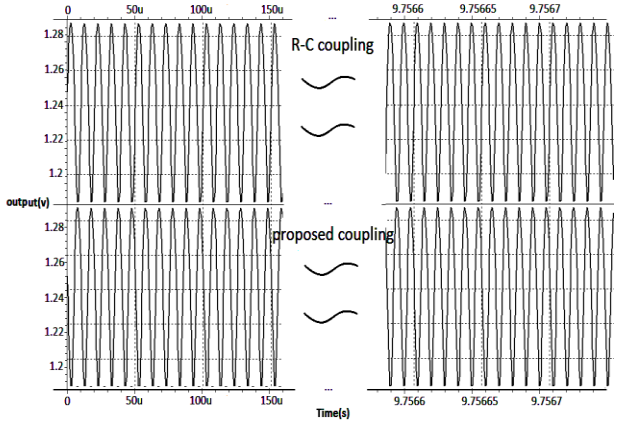


Fig. 11. Long transient simulation result of the proposed coupling and capacitive coupling

5. Conclusions

In this paper, a new coupling circuit is presented which uses a subthreshold region transistor in coupling circuit to decrease the coupling capacitor. The coupling capacitor is decreased in comparison with ordinary capacitive coupling circuit considerably. In addition, FFT simulations show that the proposed coupling achieves higher linearity in comparison with a simple capacitive coupling.

6. References

[1] N. Ghaderi, Kh. Hadidi and B. Barani, "A novel MDAC suitable for a 14B, 120MS/S ADC, using a new folded cascode OP-AMP ", *ELELIJ,* vol. *3,* no. *2,* May, 2014.

[2] M. j. M. pelgrom, A. C. J. Duinmaiger, and A. P. G. welbers, "Matching properties of MOS Transistors", *IEEE J. Solid-State Circuits*, vol. *24, ,* pp. *1433-1439,* Oct., 1998.

[3] Pui Ying Or, Ka Nang Leung, "A slew-rate enhancement technique based on current comparator and capacitive-coupled push-pull output stage for CMOS amplifiers", in *IEEE Int. Conf. on Electron Devices and Solid-State Circuits*, Hong Kong, EDSSC 2008, *2008*, pp. *1-4.*

[4] B. Razavi, "Design of analog CMOS integrated circuits", McGraw-Hill, New York, USA, 2001.

[5] Aggarwal. B, Gupta. M, "Low-Voltage Cascode Current Mirror Based on Bulk-Driven MOSFET and FGMOS Techniques", in *Int. Conf. on Advances in Recent Technologies in Communication and Computing*, Kanyakumari, ARTCom '09, 2009, pp. *473-477.*

[6] X.-G. Zhang, and E. I. El-Masry, "A regulated body-driven CMOS current mirror for low-voltage applications", *IEEE Tran. On Circuits and Systems*, vol. *51, no. 10,* pp. *571-577,* Oct., 2004.

[7] H. Yu, K. El-Sankary, and E. El-Masry, "A high-output impedance, wide swing bulk-driven current source with dynamic biasing", in *25th IEEE Canadian Conf. on Electrical & Computer Engineering, Montreal*, 2012, pp*1-4*.

[8] L. F. Tanguay, M. Sawan and Y. Savaria, "A very-high output impedance current mirror for very-low voltage biomedical analog circuits", in *IEEE Asia Pacific Conf. on Circuits and Systems*, Macao, APCCAS 2008, 2008, pp. 642 - 645.

[9] K. Ueno, T. Hirose, T. Asai and Y. Amemiya, " A 300 nW, 15 ppm/ °C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs", *IEEE J. Solid-State Circuits*, vol. *44, no. 7,* pp. *2047-2054,* Jul., 2009