A Novel Ultra High Speed and Low Power Phase Detector, Using Carbon Nanotube Field Effect Transistor

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Abstract

As the scaling of conventional silicon transistors moves towards its limiting value, designers become interested to exploit novel nano technologies. Carbon Nanotube Field Effect Transistor (CNFET) is a potential alternative device that eliminates most of physical limitations. In this paper a high speed, low power, high precision and extensive range CNFET based phase detector (PD) is presented. The sequential circuits and feedback path are omitted in the proposed PD to obtain the best speed. In addition, by employing a new method, the dead zone and missing edge problems are completely solved in the propose PD. Simulation results using HSPICE based on CNFET model show that the proposed PD consumes only 24.5µw power and is much faster compared to the previous works.

1. Introduction

In the last decades, silicon-based integrated circuit technology has experienced tremendous growth due to the scaling of device dimensions. However the size reduction of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) below a few tens of nanometers decreases their performance due to the non-ideal phenomenas such as gate oxide leakage, mobility degradation and low "ON" current[1]. Researchers currently have concentrated on CNFETs as a promising alternative of MOSFETs in the nano regime. CNFETs are novel nanoscale devices with high performance due to their premier electrical properties. Recently some circuits like opamps[1], biosensors[2], ternary memory cells[3] and SRAM cells[4] using CNFETs have been modified. It seems that CNFETs can obtain a superior "ON" current density, higher operation frequency and a considerably lower power consumption[5]. Thus, CNFETs are useful to design a high-speed circuit with low power consumption.

As the speed increases, a higher clock frequency is required. Phase-locked loops (PLLs) and delay-locked loops (DLLs) are widely used in modern communication systems to generate a clock signal which is synchronized with a reference clock. These circuits are commonly used in many applications such as clock/data recovery, frequency synthesis and phase/frequency modulation. PD is an essential functional block of PLL, which is used to detect a phase error signal and plays a key role in improving the speed of the PLL system. The outputs of PD are "UP" and "DN" signals that switch the current of a charge pump to adjust the control voltage of a voltage controller oscillator (VCO). Fig.1 shows a well-known linear PFD architecture using D-type master-slave flip flops [6]. Conventional PDs have closed loop structures because it is simple to design and doesn't have the dead zone problem. However the speed of these systems is limited due to the use of a feedback path. Furthermore some of the clock rising transitions which are overlapped with the reset signal will be missed and cannot be detected [7]. Until now some circuits have been proposed to force the feedback path faster [8][9]. However the feedback path, which causes a reduction in the speed, is still remain in all of them. Therefore by setting an open loop path and using CNFETs a high speed, high efficiency PD can be designed.

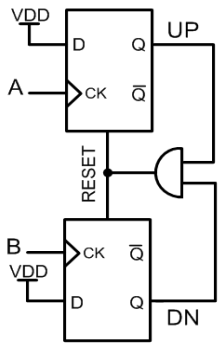

Fig. 1. Logic schematic of the conventional PD

In this paper, a simple and fast CNFET based open loop PD is presented, which detects phase difference in a wide frequency range from 1MHz to 12.5GHz. Adjustable threshold voltage (V_{th}) is one of the most exciting features of CNFETs that is used to design a simple PD with a few transistors[10]. The remainder of the paper is organized as follows. Section 2 presents a short description of the fundamental of CNFETs and introduces different kinds of them. The proposed open loop PD is discussed in Section 3. Section 4 reports simulation results and compares the proposed structure with the previous works. Finally, conclusions are provided in Section 5.

2. CNFETs

Carbon nanotubes (CNTs) are graphen strips rolled into a seamless, hollow cylinder [11]. The features of CNTs rely

strongly on physical properties like their diameter, their length and chirality (direction of the graphen sheets). For instance, by varying intrinsic bandgap CNTs can be implemented in single (SWCNT) and multiwalled (MWCNT) geometries. Also, SWCNTs could be either semiconducting or metallic based on their chirality [2]. Chirality vector is indicated by the positive integers (n_1, n_2). CNT act as metallic if $n_1 = n_2$ or $n_1 - n_2 = 3q(\mathrm{q} \in \mathrm{z})$. Otherwise, the nanotube is semiconducting [12]. The diameter of the CNT is given by [13]:

$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \approx 0.078\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad . \qquad (1)$$

Where $a = 2.49A^\circ$ is the lattice constant. CNTs have superior properties such as near ballistic transport owning to ultra long mean free path for elastic scattering [14] that make them proper candidate for use in the channel region of FETs named CNFETs[15].

In terms of the device operation mechanism, CNFETs can be divided into two groups of schottky barrier CNFETs (SB-CNFETs) and MOSFET-like CNFETs[1]. SB-CNFET is fabricated using direct contacts of the metal with the semiconducting CNTs for source and drain regions and undoped semiconducting nanotube for the channel region. These devices show a bipolar behavior that makes them unsuitable for utilizing in conventional CMOS logic families [11]. The energy barrier at the schottky barrier limits the transconductance of the CNFETs and decreases the I_{on}/I_{off} ratio [16]. In MOSFET-like CNFET, intrinsic semiconducting CNTs are placed under the gate in the channel region and heavily doped CNTs are used for the source and drain regions. They have unipolar characteristics and significantly higher Ion/Ioff ratio unlike SB-CNFETs [11]. As a result, this type of CNFETs is more suitable for ultra-high performance applications [3]. Therefore, in this paper, MOSFET-like CNFETs are employed for designing the PD. The current- voltage characteristics of CNFETs are similar to MOSFETs. So, to turn on the CNFET, a threshold voltage should be defined. The threshold voltage of the CNFET can be approximated to the first order as the half-bandgap that is proportional to the inverse of the diameter of CNT and can be expressed as[10].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}aV_\pi}{3eD_{CNT}} \approx \frac{0.43}{D_{CNT}}v \quad . \qquad (2)$$

Where *a* is the lattice constant, *e* is the unit electron charge, and $V_\pi = 3.3ev$ is the carbon $\pi - \pi$ bond energy in the tight bonding model. This geometry-dependent threshold voltage has been used to obtain CNFETs that turn on at different voltages relying on their diameters.

3. Proposed CNFET based PD

Until now, various close-loop and open-loop PDs have been implemented in different logic styles [17-20]. Although these structures tried to solve the dead zone and missing edges problems of PDs, but they couldn't significantly improve the operation frequency and power consumption. All of the previous PDs are implemented using different kinds of CMOS technology.

In this section a novel open loop PD with high operation frequency and low power consumption based on carbon nanotube technology is going to be illustrated. As shown in Fig. 2, the proposed design is constructed in three stages. The first stage generates a signal which is a complement of the lagged input ($\overline{Lag}$) using two capacitors and two CNFETs. According to the input signal values, the capacitors produce 3 logic levels, 0, VDD/2 and VDD at the gates of T_1 and T_2 (G_1 node) . The threshold voltages of T_1 and T_2 are regulated as follows. The "$\overline{Lag}$" signal will be high when both of the inputs are low (logic level = 0) and it will be low if both of the inputs are at the high value (VDD level). At the rest of the input states, the output doesn't change. For better evaluation, the different states are tabulated in Table 1.

Table 1. Different states of the first segment of the Proposed PD

A	B	Logic level of G_1	T_1	T_2	Lag not
0	0	0	Off	On	1
1	0	VDD/2	Off	Off	Previous state
1	1	VDD	On	Off	0
0	1	VDD/2	Off	Off	Previous state

The second stage implements "$\overline{UP}$" and "$\overline{DN}$" by using two NAND gates. "$\overline{UP}$" will be set to zero when both of its inputs ("$\overline{Lag}$" and A") are high. Otherwise it will become high. "$\overline{DN}$" signal is generated in a similar manner. Finally, two inverters is needed to implement "UP" and "DN" signals with sharp edges, which are used in the charge pump circuit to produce a voltage or current as a control signal to VCO. Just 10 transistors have been used to design the proposed PD that is unprecedented compared to the previous works. In addition, these transistors are much faster and consume less power in comparison with MOSFETs. According to Eq. (2), the diameter of each transistor is computed and written in Fig. 2.

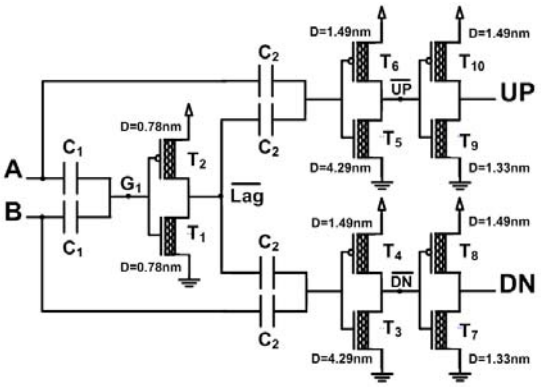

Fig. 2. Proposed CNFET based PD

Producing of "UP" and "DN" signals is illustrated in Fig. 3. Initially, both "A" and "B" signals are set to minimum value

("A=0 and B=0"). Therefore according to Table 1, "$\overline{Lag}$" signal is set to VDD level and subsequently, "UP" and "DN" signals will be zero. When the rising edge of "A" occurs, "$\overline{Lag}$" and "DN" signals will remain at the previous state and "UP" signal will be set to the high value. After the rising transition on "B", T_3 will turn on and "DN" signal will be set to the high level.

After a specific time delay, the "$\overline{Lag}$" signal will change its state. This time delay is produced due to the capacitors in the proposed structure, which is needed to produce "DN" signal and earn enough time for output signals to reach a logical level in small phase differences. "UP" and "DN" signals will be set to "0" when the falling edge of "$\overline{Lag}$" happens. As it is shown, "UP" and "DN" signals overlap with each other, which makes equal charge and discharge currents pass through the filter capacitor. In this way the dead zone of the proposed structure will be zero that is very desirable for high speed systems. In the previous open loop structures [20], the delayed version of the input signals have been used to overcome the dead zone problem. However, adding delay element imposes some additional circuits and also enhances the jitter and mismatch problems at the output pulses of VCO. As mentioned above, in the proposed circuit, discharging time of the capacitors, which is proportional to their time constant, is used to makes a constant signal overlap and eliminates the above problems.

At the next step, "A" becomes zero while "$\overline{Lag}$" remains in the previous state. Then "B" goes low and "$\overline{Lag}$" will be set to "1".

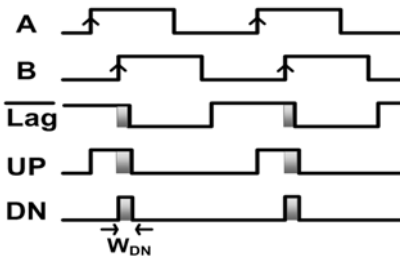

Fig. 3. The waveforms of the proposed PD

As it was mentioned, the pulse width of "DN" signal (W_{DN}) is related to the discharging time of the "$\overline{Lag}$" node capacitance (Fig. 4). "UP" and "DN" signals remain at their previous states until the voltage of G_3 and G_5 nodes reduce less than the threshold voltages of T_3 and T_5. Then they will turn off and "UP" and "DN" signals will be set to zero. The discharge time and subsequently "W_{DN}" is estimated as fallows. As it is shown in Eq. (3), the drain-source resistance of T_1 is approximately equal to the resistance of CNTs which are placed in the drain, source and channel regions. The capacitance of T_1 is negligible in comparison with the connected capacitors (C_2). The equivalent capacitance at the "$\overline{Lag}$" node is equal to 0.5fF. The time which is needed to discharge the "$\overline{Lag}$" node capacitance from VDD to 0.368 VDD is equal to the value of time constant (τ) (Eq. (3)). This time is needed to turn off T_3 and T_5 and turn on T_4 and T_6.

$$R_{eq} \approx \frac{R_{CNT} * 96nm}{Tubes}, R_{CNT} \approx 3.3\frac{K\Omega}{\text{nm}}, \text{Tubes} = 5 \rightarrow R_{eq} = 63.36K\Omega,$$
$$C_{eq} \approx C_{eq1} \| C_{eq2}, C_{eq1} = C_{eq2} \approx \frac{C_2}{2} = 0.25fF \rightarrow C_{eq} \approx 0.5fF,$$
$$W_{DN} \approx \tau, \text{Where } \tau = R_{eq} * C_{eq} \rightarrow W_{DN} \approx 31.68ps. \quad (3)$$

In the above equation, Tubes is the number of CNT tubes in the device, R_{eq} and C_{eq} are the equivalent resistance and capacitance of "$\overline{Lag}$" node, respectively.

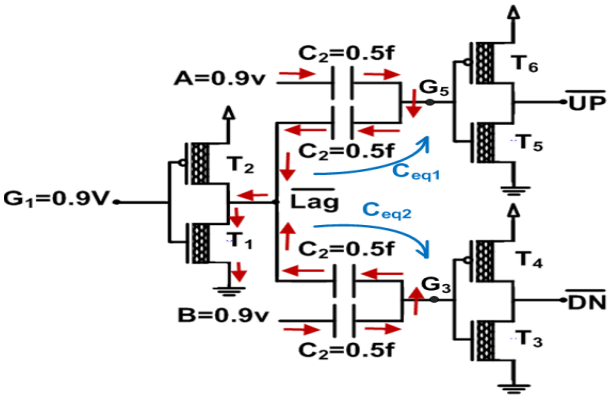

Fig. 4. The discharge paths of the $\overline{\text{lag}}$ node, which are shown with red vectors

4. Simulation Results and Design Comparison

The HSPICE circuit simulator has been used to simulate the proposed PD. The standard model presented in [16] has been used to simulate enhancement-mode unipolar MOSFET-like CNFETs, in which each transistor may include several CNTs as its channel. The important parameters of the top gate CNFET standard model are physical channel length (L_{ch}=32nm), the length of doped CNT source-side extension region (L_{ss}=32nm), the length of doped CNT drain-side extension (L_{dd}=32nm), the width of metal gate (W_{gate}=6.4nm), the distance between the centers of two adjacent CNTs within the same device (Pitch=20nm), the number of tubes in the device (Tubes=1), the thickness of high-k top gate dielectric material (T_{ox}=4nm), the dielectric constant of high-k top gate dielectric material (K_{gate}=16), the coupling capacitance between the channel region and the substrate (C_{sub}=20pF/m), which are shown in Fig. 5. The default value of each parameter is written in parenthesis.

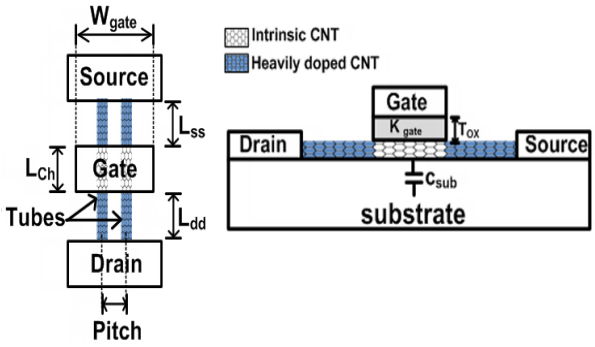

Fig. 5. Presentation of modeled CNFETs and relevant parameters

The proposed PD is simulated at room temperature and 0.9 volt supply voltage. SPICE simulation results in Fig. 6 show that "UP" and "DN" signals are made with high accuracy, while the operation frequency is very high. The pulse width of "DN" is about 29.7ps, which is approximately equal to what was theoretically estimated (31.68ps). "UP" and "DN" signals overlap with each other and simultaneously come down. In this way the dead zone will be zero, which makes it suitable for applications with high-speed and high-accuracy. Assuming that "A" and "B" signals have similar frequencies ($F_A = F_B$) and their duty cycle is 50%, the maximum frequency (F_{max}) of the inputs should be chosen so that the pulse width of them be greater than the pulse width of "DN" signal (W_{DN}). If F_{max} be more than what was mentioned and the phase difference of the inputs be close to 180^0, the DN signal does not have enough time to change its state. Therefore, Maximum frequency is given by:

$$F_{\max} = \frac{1}{2 * W_{DN}} = \frac{1}{2 * 29.7ps} = 16.8GHz \quad . \qquad (4)$$

To ensure that the circuit works properly, the operating frequency is selected 12.5GHz, which is less than maximum frequency that theoretically determined.

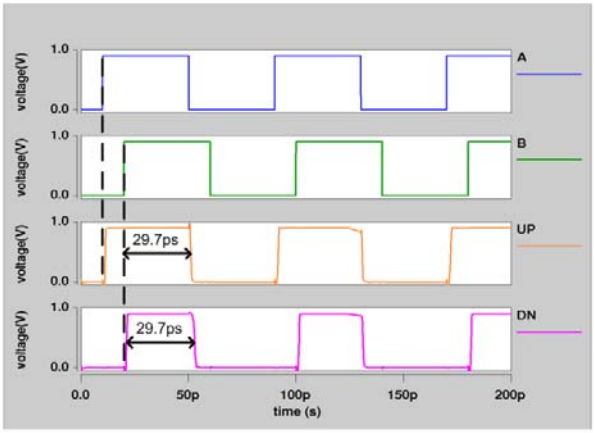

Fig. 6. The waveforms of the designed PD for an input frequency of 12.5GHz and the two inputs are 45^0 out of phase.

The input, output (I/O) characteristics of PD at frequencies of 3GHz, 10GHz, 11.1GHz and 12.5GHz are displayed in Fig. 7, where the *x* axis illustrates the phase difference of "A" and "B" signals and the *y* axis represents the average values of the difference between "UP" and "DN" signals. The region around zero, where surrounded by the circle, shows that PD behaves linearly in small phase differences even at very high frequencies (12.5GHz). Therefor, the proposed structure has low jitter, after locking of the PLL. As the phase difference increases, the transitional curves become nonlinear, but they hold correct polarity. This structure can detect phase difference in a wide frequency range from 1MHz to 12.5GHz and consumes only 24.5µw when working at 12.5 GHz.

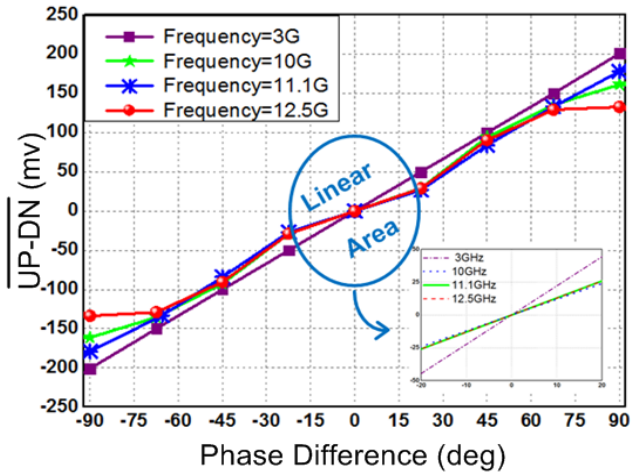

Fig. 7. I/O characteristics of the proposed PD

For highlight the advantages of the proposed PD, a comparison with the previous works is done in Table 2. As it is shown, the operation frequency is 5.95 times faster than Ref. 17, which has the best speed among previous PDs. It is 6.25 and 125 times faster than Ref. 18 and Ref. 19, respectively. On the other hand, the average power dissipation of the proposed PD is less than all of the previous structures. Therefore not only the power consumption is reduced but also the speed is increased.

Table 2. Proposed PD performance summery and comparison

References	Technology	Structure	Power	Max Freq.
Ref. 17	CMOS 130nm	Open loop	N.A	2.1GHz
Ref. 18	CMOS 130nm	Close loop	37µw @1GHz	2GHz
Ref. 19	CMOS 350nm	Open loop	16.5mw@100MHz	100MHz
This work	CNT 32nm	Open loop	24.5µw@12.5GHz	12.5GHz

5. Conclusions

In this paper, a novel low-power open loop PD has been proposed. The PD uses CNFETs and capacitors as substructure, resulting in a considerable improvement in the speed and power consumption. By omitting the delay element, a constant signal overlap is obtained, using the discharging time of the capacitors. Therefore, The proposed PD can detect very small phase differences with high accuracy and solve the dead zone and missing edge problems completely which makes it preferable

for fast lock, low output jitter and high operating frequency PLLs.

Simulation results show that the operating frequency of the presented CNFET based PD ranges from 1MHz to 12.5GHz and it consumes only 24.5µw at 12.5GHz.

6. References

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