Wideband common gate LNA with novel input matching architecture

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Abstract

In this paper, a novel architecture for wideband input impedance matching consisting of two common gate (CG) transistors is presented. One CG transistor is placed on top of the other in a current reuse fashion such that both transistors appear in parallel at the input. As a consequence, the transconductance requirement for input matching from each NMOS transistor is reduced to half compared to a simple CG LNA. The proposed input matching technique has been used to design an UWB LNA simulated using IBM 130nm CMOS process with Spectre RF. The proposed architecture accomplish large bandwidth and high gain with comparatively small power consumption. Post Layout simulation results depict S11 and S22 well below -6.5 dB and -15 dB respectively. The gain and 3 dB bandwidth are 15 dB and 2.1 GHz respectively. The LNA demonstrates minimum NF of 3.7 dB @ 3.53 GHz in the passband, input referred 1dBCP of −15.32 dBm with IIP3 of -10.5 dBm. The proposed LNA consumes only 1.87mA from 1.4V power supply.

1. Introduction

The UWB technology with a frequency spectrum from 3.1-10.6 GHz has emerged as one of the most popular, most researched and most promising wideband technology after being declared commercial by the Federal Communications Commission (FCC) in 2002. The extremely high data rate together with large bandwidth, high protection, low cost and low power makes it a suitable choice for various wireless communication applications including IrDA, Wireless USB, Bluetooth, Z-Wave, ZigBee, Body Area Network etc. Besides, UWB has also been widely used in Biomedical applications and vehicular tracking systems.

UWB LNA design is a great challenge because the stringent requirements of good input and output matching, reverse isolation, flat and high gain, low noise figure, and high linearity shall all be met over a very large frequency spectrum. Published literature is full of UWB LNAs implemented using the ever shrinking CMOS technology [1-4] which has achieved f_T as high as 280 GHz (45nm CMOS) [5].

While CG topology has been successfully used as an input matching stage for the UWB LNA, design with Common Source (CS) topology is usually avoided as this topology generally exhibits a narrowband performance. Obtaining wideband response with this topology requires additional reactive components placed before the CS transistor which actually serve as bandpass filter [4][6]. Additionally, the noise characteristics of a CS based LNA vary directly with frequency, thereby increasing Noise Figure (NF) at higher frequencies. Further, the interdependence of input and output in a CS LNA due to Miller's effect, often need the addition of a cascode stage which requires more voltage headroom thereby increasing power. The CG LNA, on the other hand, has excellent reverse isolation properties inherently. It has a slightly higher but relatively constant noise figure independent of both the operating frequency and bandwidth [1-3]. Its input capacitance C_{gs} is easily resonated out by adding an inductor at its source while its transconductance helps to fix the 50Ω input impedance match. These features makes the CG LNA superior in performance compared to CS LNA when it comes to wideband operation. A CG LNA work without a band pass filter at the input thereby saving area and makes the LNA design more simpler. In a conventional CG LNA, width of input CG MOS and power consumption are governed by the transconductance required for input matching. In this LNA, g_m of 20 mS is theoretically required from the input transistor for input matching whereas values of 22-23mS are usually set to cater for reflection of load impedance at the input [1]. The high power consumption associated with this transconductance value can be restricted using current reuse techniques which have proved to be very efficient for low power designs [7-8]. To design a low power CG LNA, we propose a new input matching architecture with the goal to use lesser current and achieve a comparable gain as in standard CMOS CG LNAs. In our proposed design, one CG transistor is placed at the top of other such that the sum of transconductances of both transistors provide the desired 50Ω matching. Thus input matching is possible at approximately half the transconductance/ current consumption value compared to conventional CG LNA. The proposed LNA achieves comparable bandwidth, gain and noise figure with low power compare to previously reported LNAs.

The paper is divided as follows. In section 2, main design concept, mathematical equations and circuit parameters are presented. Layout design and post layout simulation results are presented along with comparison with recent LNAs in section 3 and the paper is finally concluded in Section 4.

2. Circuit Design

2.1.Design theory

Fig. 1 shows the schematic of the proposed LNA design. In the input matching stage, capacitors C_1 and C_2 couple the input signal to the sources of CG transistors M_1 and M_2. M_2 is stacked at the top of M_1 which allows both M_1 and M_2 to share the same

drain current. Both M_1 and M_2 act as input impedance matching device and their input impedance appear in parallel at the input of the LNA as in (1). The input impedance of either M_1 or M_2 consists of inverse of sum of respective transconductance (g_{m1} for M_1 and g_{m2} for M_2) and the gate to source capacitance (sC_{gs1} for M_1 and sC_{gs2} for M_2) present at the source node. The inductors L_1 and L_3 placed at the sources of M_1 and M_2 resonate out sC_{gs1} and sC_{gs2} respectively as in simple CG LNAs. As a result, the real part of input impedance looking into the LNA is equal to inverse of the sum of the transconductances of M_1 (g_{m1}) and M_2 (g_{m2}) only. This resistive component is used to match the LNA input impedance to the source resistance (2)-(3).

$$Z_{in} = Z_{in1} \| Z_{in2} \quad (1)$$

$$Z_{in1} = \frac{1}{g_{m1} + sC_{gs1} + \frac{1}{sL_1}} \quad (2)$$

$$Z_{in2} = \frac{1}{g_{m2} + sC_{gs2} + \frac{1}{sL_3}} \quad (3)$$

where Z_{in} is the total input impedance of the LNA, Z_{in1} and Z_{in2} are the input impedances looking into the source of M_1 and M_2 respectively. g_{m1}, g_{m2} and sC_{gs1}, sC_{gs2} are the transconductances and gate to source capacitances respectively of M1 and M2. sL_1, sL_3 are the impedances of L_1, and L_3 respectively. As C_{gs1} is resonated out by L_1, and C_{gs2} by L_3, Z_{in} is effectively equal to $Z_{in} = 1/(g_{m1} + g_{m2})$.

The gates of M_1 and M_2 are kept at ac ground with the help of C_3 and C_6 as this further improves the input impedance matching. Inductors L_2 and L_4 serve as the load for M_1 and M_2 respectively and carry the same bias current. The combination of inductors L_2, L_3 and capacitor C5 make a third order LC-T network and provides adequate isolation between both M1 and M_2. Capacitor C_5 also presents an ac ground over the entire bandwidth of interest. The RF signal after amplification through M_1 and M_2 is coupled through C_4 and C_7 to the gain stage comprising of M_3 and M_4 again in a current reuse fashion. This stage provides additional gain to the LNA. Besides current reuse, the placement of PMOS and NMOS in an inverter configuration also helps to improve the linearity which depends on latter stage of the LNA. The output of this stage is coupled through C_8 to the buffer stage. This capacitor also isolates the dc biasing between gain stage and the buffer. The series resonance of this capacitor with inductor L_5 and further resonance of L_5 with the input capacitance of M_6 assist in extending the bandwidth towards higher frequency spectrum of the desired band. The gain (A) of the LNA can be expressed as in (4).

$$A = -(r_{01} \| r_{02})(g_{m1} g_{m3} sL_2 + g_{m4} g_{m2} sL_4) \quad (5)$$

where r_{01} and r_{02} are the drain to source resistances of M_1 and M_2 respectively. g_{m3}, g_{m4} are the transconductances of M_3 and M_4 respectively. sL_2 and sL_4 are the impedances of L_2 and L_4 respectively. Noise Figure for the proposed LNA can be written as in (5).

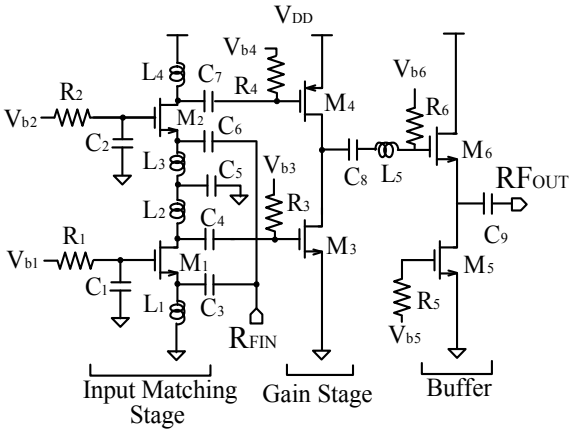

Fig. 1. Proposed current reuse common gate LNA with novel input impedance matching architecture

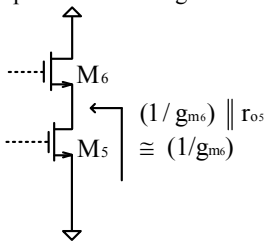

Fig. 2. Figure showing how output impedance of 50 Ω is obtained through buffer

$$NF = 1 + \frac{\gamma}{\alpha g_{m1} R_S} + \frac{\gamma}{\alpha g_{m2} R_S} \quad (5)$$

where noise of the gain stage has been neglected according to Frii's formula. In (5), γ is a noise parameter (coefficient of channel thermal noise) for deep submicron MOSFETS and its value can be much greater than 1 for short channel devices. $\alpha \cong gm/gd0$ and its value can be much less than 1 for short channel devices [9]. M_5 and M_6 implement the buffer for the proposed LNA which is mainly added to assist in output matching. The inverse of transconductance of M_6 ($1/g_{m6}$) and the output impedance of M_5 (r_{05}), appear in parallel at the output node of the buffer, hence at the output of the LNA. By adjusting g_{m6} to match the 50 Ω output impedance of cable and a high r_{05} for M_5, the parallel combination of $1/g_{m6}$ and r_{05} reduce to $1/g_{m6}$ only shown in Fig. 2. In this way, output impedance matching is achieved through the buffer.

The gate bias of all transistors is provided through current mirrors. Input matching stage is biased at a current of 0.53 mA while gain stage carries a bias current of 1.34 mA. Buffer is biased separately with a power supply of 1 volt.

2.2.Circuit Parameters

From (1), g_{m1} and g_{m2} should be 10mS each ideally, and the simulations are started with this value. After rigorous simulations and keeping in view the requirement of low power consumption, the transconductance values are adjusted to g_{m1} = 9.3mS and g_{m2} = 8.3mS respectively by setting M_1 and M_2 for gate widths of 40µm and 30µm respectively. With these values, S_{11} values as low as -15dB are obtained in passband. Increasing

gm's above the aforementioned values only increase power consumption without much difference in S_{11}. Hence above values are retained.

Inductors L_1, L_3 are selected to be 7.6 nH each and they resonate with gate to source capacitances plus other parasitic capacitances present at the source nodes of M_1 and M_2 respectively to create resonances at lower end of frequency spectrum near 3.8 GHz and 4.5 GHz (pre-layout simulation). L_2 appear at the drain of M_1 and at the gate of M_3 while L_4 is at the junction of drain and gate of M_2 and M_4 respectively. Iterative simulations are done after which desired gain is obtained for widths of M_3 and M_4 as M_3 = 85µm and M_4 = 110µm while L_2 = 8 nH, L_4 = 6.6 nH and L_5 = 7.6 nH. These component values are chosen to obtain a wideband gain response by creating multiple resonances in the desired spectrum. Buffer transistors width are adjusted as M_5 = 31µm and M_6 =20.9µm to facilitate output matching already discussed in Section II.A above. The total power consumption of LNA core is 2.61 mW from a 1.4 V supply. The gate bias values of M_1 through M_6 are V_{b1}=V_{b3} = 0.45V, V_{b2} = 1.4, V_{b4} = 0.84V, V_{b5} = 0.44V, V_{b6} = 1V.

3. Simulation Results And Layout

The Layout of the proposed LNA is presented in Fig. 3 having an area of about 0.74 mm^2 (1.1 x 0.67 mm^2) excluding bondpads. The LNA layout is designed in Cadence Layout XL using 0.13 µm CMOS technology by IBM. DRC, LVS, QRC, floating gate, Orthogonality tests and post layout simulations have been successfully performed on the LNA layout. Fig. 4 through Fig. 9 present the pre and post layout simulation results for the LNA. It can be seen that due to the presence of parasitics in the Layout and due to the insertion of tie down diodes at various nodes, the post layout simulation results are greatly deteriorated. Fig. 4 and 5 present the input and output reflection coefficient for the LNA respectively. While post layout S_{11} remains below -10 dB from 2.6-4 GHz, S_{22} remains below -15 dB throughout the bandwidth of interest. In fig. 6, power gain of the LNA is presented. The pre-layout simulation shows a maximum gain value of 15 dB and 3 dB bandwidth of 4GHz (2.5-6.5 GHz) whereas the bandwidth reduces to 2 GHz after post layout simulation. Thus, the effective bandwidth for the LNA exists from 2.3-4.4 GHz. Also, not shown is the reverse isolation of the LNA which remained below -50 dB in both pre and post Layout simulation results. The noise figure of the LNA is shown in Fig. 7. The minimum NF achievable in the passband is 3.7 dB while average NF is 5.3 dB from the post layout results. Linearity tests on the LNA gives 1 dB compression point to be -15.32 dBm as shown in Fig. 8. Two tone test on the LNA is performed using tones of 3 GHz and 3.01 GHz which determines the input referred third order intercept point to be -10.5 dBm as shown in Fig. 9.

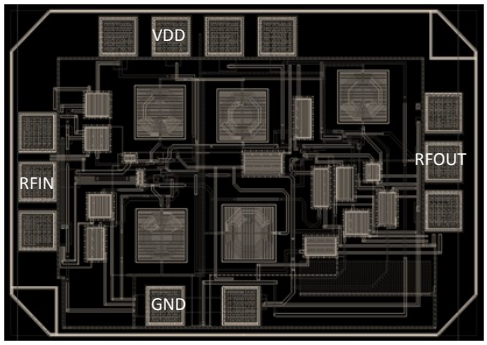

Fig. 3. Layout of the proposed LNA with an area of 1.1 x 0.67 mm^2 excluding bondpads

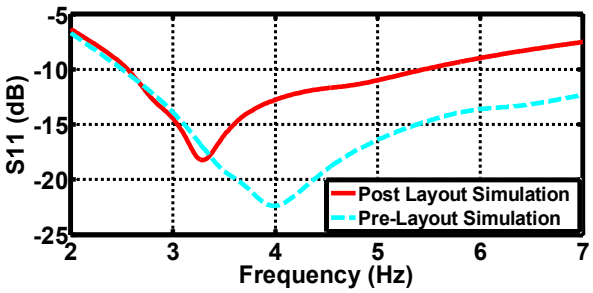

Fig. 4. Pre and Post Layout Simulated Input Reflection Coefficient of the LNA

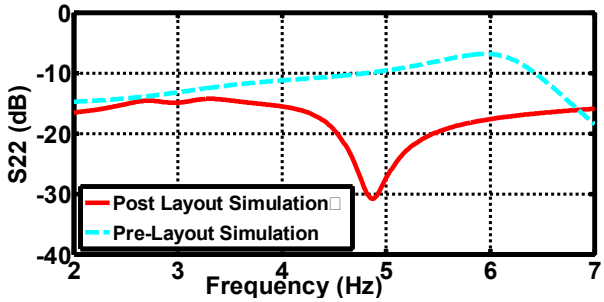

Fig. 5. Pre and post layout simulated output reflection coefficient of the LNA

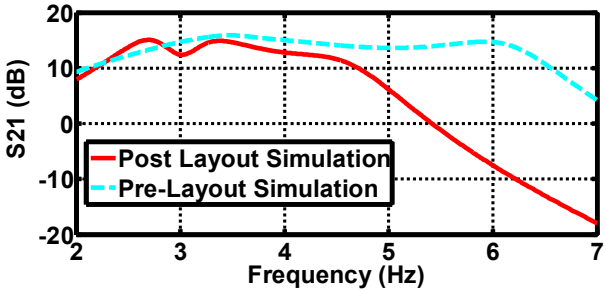

Fig. 6. Pre and post layout simulated power gain of the LNA

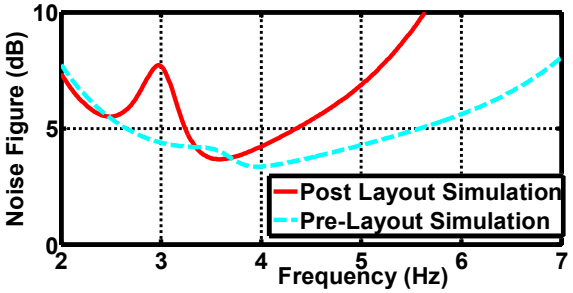

Fig. 7. Pre and post layout simulated Noise Figure of the LNA with minimum NF of 3.7dB @ 3.53 GHz

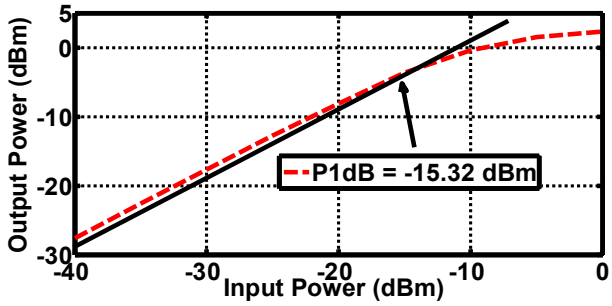

Fig. 8. Simulated input referred 1 dB Compression Point (−15.32 dBm)

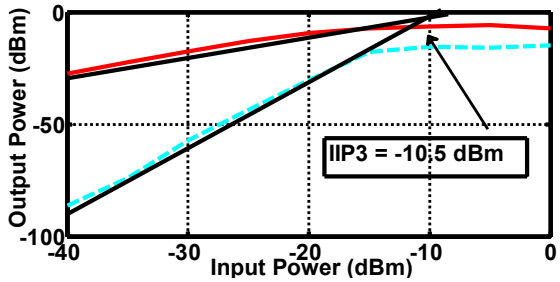

Fig. 9. Simulated input referred third order intercept Point (−10.5 dBm)

Table 1. Performance Comparison Of The Proposed LNA

Ref no.	[1]	[8]	[10]	[11]	[12]	[13]	This work
Tech (nm)	130	130	180	180	65	180	0.13
Freq (GHz)	3.1-4.8	0.8-2.1	0.02-1.18	0.3-0.92	0.2-5.2	3-4.8	2.3-4.4
S11 (dB)	<-8	≤-6	≤-10	≤-10	<-14**	<-10	-6.5
Gain (dB)	13	14.5	20.5	21*	15.6*	15	15
NFmin (dB)	3.5	2.6	3.3	2	2.9**	3.5	3.7
IIP3 (dBm)	-6.1	+16	2.7	-3.2	3.9**	N/A	-10.5
Power (mW)	3.4	17.4	32.4	3.6	14	5	2.6

*voltage gain **estimated from graph

Table-1 compares the performance of our proposed LNA with other reported LNAs designed in comparable technology nodes and having similar specifications. Our proposed LNA offers much larger bandwidth and gain with smaller power consumption.

4. Conclusions

The paper presents the design of a new common gate based input impedance matching architecture employing current reuse technique. Each CG NMOS of the matching stage has been biased at almost half the transconductance compared to a conventional common gate LNA, thus reducing the overall power consumption. Post Layout simulation results present S11< -6.5 dB, S22< -15 dB, maximum gain 15 dB, average NF of 5.3. Input referred P1dB and IIP3 are -15.32 dBm and -10.32 dBm respectively. The proposed LNA achieves high gain, wider bandwidth with smaller power consumption. Large bandwidth with low power makes it an appropriate option for wideband receivers in handheld/ battery operated devices.

5. References

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